

1V DSP IN WIRELESS COMMUNICATION SYSTEMS

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ABSTRACT: The requirements of the rapidly expanding second and third generation mobile communication systems place increasing demands on DSP algorithms and their implementations. This paper presents a survey of the implications of the new cellular system technology on the DSP functionality and implementation of 1V DSP processors for mobile systems. Modern cellular phones are placing increasingly stringent demands on battery life and, therefore, on the power dissipation of the embedded DSP circuitry.

At the same time, greater computational throughput is being required of the DSP, for example to implement more sophisticated speech and channel coding algorithms. Earlier low-power DSPs have been reported. However, further improvements in power and performance are required. As is well known, the demand for wireless communications has been steadily increasing in recent years and the number of subscribers in wireless systems is expected to grow also in the future.

Key Words: DSP, 3G, 4G, Wireless Communication.

I. INTRODUCTION

Digital signal processing has emerged as one of the key technologies in implementing the new communication systems. The increasing service requirements of the wireless cellular communications require efficient modulation, coding and control algorithms. The growing algorithmic complexity on one hand and the rapid price erosion of particularly the terminal equipment on the other hand are in turn placing stringent requirements on the implementation technology. The new system specifications often contain built-in expectations of steady development in the performance/price ratio of microelectronic devices. Our main topics in this paper are the effects of the new system requirements on the algorithmic complexity on the terminal and base station equipment as well as the current and expected future implementation complexity in relation to the recognized trends in the microelectronics industry. When discussing system details, specific algorithms and their implementations, our emphasis is on the cellular communication systems developed in Europe.

II. WIRELESS COMMUNICATION SYSTEMS

The entire class of wireless communication systems is very wide, including such diverse items as personal cellular and cordless communications systems (e.g. NMT, GSM, DECT), paging systems (e.g. ERMES), trunked radio systems (e.g. TETRA), satellite radio systems (e.g. INMARSAT), airtoground passenger telecommunications (TFTS) and wireless LANs (e.g. HIPERLAN). In this paper we concentrate on the personal communication systems having the greatest impact on the global market of telecommunications. Currently the wireless personal communication systems can be divided in the categories of cellular and cordless systems, but in the future this distinction may be removed. The former category is often classified into the first-, second- and third- generation

cellular systems. The first generation is represented by analog systems such as NMT or TACS, while the second generation includes among others the current digital GSM, DCS; JDC and U.S. TDMA and CDMA systems. Extensive research efforts are currently being targeted on third-generation systems like the European UMTS (Universal Mobile Telecommunication System). UMTS is based on the ITU's FPLMTS (Future Public Land Mobile Telecommunication System) framework and operates within FPLMTS frequencies. The cellular systems are characterized by the support of terminal mobility by call hand-over between the base stations of the network. The cordless systems such as CT2 or DECT, on the other hand, offer only limited coverage by either personal or low-power public base stations.

The analog first-generation cellular systems provide only a basic voice communication service using frequency modulation with frequency division multiple access method. The implementation of the terminal and base station equipment is also relatively simple. The systems are national or regional (NMT operates in several countries including all the Nordic countries).

The services provided by the second generation systems, especially GSM/DCS, are considerably more versatile. Besides inherently larger system capacity, GSM offers various voice coding options, various data transmission possibilities as well as powerful signalling. As a global system defining not only an air interface but a complete network, GSM currently allows for roaming across a large number of countries. GSM uses a time division multiple access method combined with a slow frequency hopping scheme and depends heavily on digital signal processing implementations.

Third generation systems, such as the European UMTS aim to offer still a considerably wider variety of services, many of them wireless extensions of ISDN. UMTS is also compatible with the ATM (Asynchronous Transfer Mode) though the current B-ISDN standards cannot support a mobile system like UMTS [3]. UMTS offers for example several alternative speech codec's at 2 to 64 kbits/s and families of picture, video and data codec's as well as advanced data protocols. The new system features and overall architecture of the third generation system are needed to provide cost efficiency, flexibility and capacity for the implementation of high bit rate services and global roaming. The future systems will support true mobility in which a single terminal can be used regardless of the environment utilizing different infra-structure subsystems. Advanced versions of TDMA and CDMA access have been studied for flexible multiple access in these systems. The implementation of a full third generation communication system will raise the requirements on DSP technology to a completely new level.

III. DSP ARCHITECTURES FOR 3G MOBILE COMMUNICATIONS SYSTEMS

The choice of a DSP to obtain the required computation speed is not a direct matter of specifying the highest clock speed Architecture and instruction sets greatly affect the speed of algorithm execution. "MIPS" (millions of instructions per second). Another aspect to consider is the class of DSP architecture employed.

Two recently introduced new classes to consider are: very long instruction word (VLIW) and static superscalar .VLIW tries to reduce cost and increase execution speed by reducing hardware complexity. The sequencing mechanism in VLIW depends on an instruction format. In VLIW, all operation latencies in a particular implementation are fully open to software. The TMS320C6x series from Texas Instruments is an example of VLIW architecture. Static superscalar architectures apply a consistent and functionally well-defined programming model, and the schedule is determined prior to run time. The Tiger SHARC™ DSP from Analog Devices is an example of a static superscalar architecture.

IV. REDUCING POWER CONSUMPTION TO 1 V

All kinds of mobile communications terminal equipment are characterized by the requirements of small size, light weight, and battery based operation over long periods. These called for low power consumption. Most of the power in a mobile phone is drawn by its RF section, particularly the power amplifier. However, the power consumption of the DSP section is not negligible and it is actually quite important during periods when the RF section is not transmitting.

Improvements in the silicon technology, has the advantage reduction in the power operability. The current standard portable electronics is 3.3 V. The technology limit has been forecast to go down to about 1 V by the next decade. Reduction in feature sizes also lowers power consumption, which is primarily due to smaller capacitances. Modern cellular phones are placing increasingly stringent demands on battery life and, therefore, on the power dissipation of the embedded DSP circuitry. At the same time, greater computational throughput is being required of the DSP, for example to implement more sophisticated speech and channel coding algorithms. Earlier, the low-power DSPs have been reported. However, further improvements in power and performance are required.

The CPU uses a modified Harvard architecture as shown in Figure 1. To maximize throughput, the CPU employs a six-stage instruction pipeline. Three separate data buses and one program bus coupled with two data and one program address generator facilitate a high degree of parallelism. This result in a highly efficient instruction set that in turn increases the energy efficiency of the processor. The CPU contains a 40b &U that can selectively feed one of two 40b accumulators. By setting a status register bit, the ALU can function as a single unit or as two 16b &U's operating in parallel. The DSP features a multiply-accumulate (MAC) block capable of a 17x17 multiplication and a 40b addition in a single cycle. The MAC and ALU can operate in parallel. This DSP also contains a compare, select, and store unit that accelerates the Viterbi butterfly computation required by many communication algorithms. The on-chip memory subsystem includes 6kx16b SRAM and 48kx16b ROM divided into separate program and data

spaces. In addition to the CPU and memory, on-chip peripherals include a timer, two serial ports, and an 8b parallel host interface.

The DSP uses an on-chip PLL for clock generation that can be driven either by an external clock. The choice of a DSP to obtain the required computation speed is not a direct matter of specifying the highest clock speed Architecture and instruction sets greatly affect the speed of algorithm execution. "MIPS"(millions of instructions per second). Another aspect to consider is the class of DSP architecture employed. Two recently introduced new classes to consider are: very long instruction word (VLIW) and static superscalar .VLIW tries to reduce cost and increase execution speed by reducing hardware complexity. The sequencing mechanism in VLIW depends on an instruction format. In VLIW, all operation latencies in a particular implementation are fully open to software. The TMS320C6x series from Texas Instruments is an example of VLIW architecture. Static superscalar architectures apply a consistent and functionally well-defined programming model, and the schedule is determined prior to run time. The Tiger SHARC™ DSP from analog devices is an example of a static superscalar architecture. Programmable frequency dividers in the feed forward and feedback paths allow clock multiplication by 31 possible ratios ranging from 0.25 to 15. To facilitate operation at 1V, the traditional analog charge-pump, loop filter, and VCO circuitry have been replaced with a digital loop filter and a digitally-controlled oscillator (DCO). The DCO shown in Figure 2 uses a binary weighted switched-capacitor array to produce a loading on the variable delay stage that is roughly proportional to the digital input. The capacitors are implemented as nMOS transistors, that can be deactivated by driving their source/drain connection to Vdd, placing the transistor in the depletion region of operation and greatly reducing its gate capacitance. The result is a DCO whose period of oscillation is linearly related to the digital input

$$T = T_{\text{offset}} + (d_0 \cdot 2^0 + d_1 \cdot 2^1 + \dots + d_n \cdot 2^n) T$$

During active operation of the DSP, power savings are realized by extensive use of gated clocks (Figure 3). In particular, latches are only clocked when useful data is available at their inputs. This is achieved by locally gating the master clock with a data ready signal. This signal is generated by local control logic using

Information from the instruction decoder. The gated slave logic registers that data has been clocked into the master latch, and outputs an enable signal that gates the slave clock. Thus, functional blocks are only activated when they have valid data to process. Global clock gating is also available and is controlled by three power-down instructions: IDLE1, IDLE2, and IDLE3. The IDLE1 instruction shuts down the CPU, the IDLE2 instruction shuts down the CPU and the on-chip peripherals (however the PLL remains active), and the IDLE3 instruction shuts down the entire processor.

The memory subsystem allows two data operand reads from any one of the three 2kx16b on-chip SRAM blocks in a single machine cycle. Divided word line architecture is used in the SRAM to reduce power. Each 2kx16b SRAM block is divided into two banks as shown in Figure 4. The banks in turn are sub-divided into four 256x16b arrays, each with its own local word line driver. Consequently, each memory access only activates 1/8 of the entire array, thereby reducing

the power consumption. High V_t transistors are used in the six-transistor memory cell to keep the standby current I_{off} a minimum, while low V_t transistors are used in the sense amplifier and all peripheral circuitry to allow for high speed operation at 1.0V and below. The program and data store ROMs on this chip utilize selective precharge of bit lines, for essentially zero standby power dissipation and low operating power consumption. The diffusion-programming feature results in a 40% memory array area savings with respect to via- or contact-programmed cores of the same capacity. Area reduction lowers bit line and word line capacitance and, thus, power.

The chip uses a 0.35 μ m (0.25 μ m gate length) dual- V_t , twin-well, triple-metal CMOS process and measures 5.65x5.50mm².

The dependence of speed and power consumption on supply voltage is shown in Figure 5. The chip reaches 63MHz at 1.0V and 100MHz at 1.35V. The chip is functional down to 0.6V. At 1.0V and 63MHz, the power dissipation while running an FIR filtering application is 17.0mW for the core (power dissipated by the I/O pads is excluded). The power-performance metric of the processor is 0.21mW/MHz. This is the slope of the powers. Frequency graph and, therefore, only accounts for dynamic power. Due to extensive use of low V_t transistors, the standby power is quite high at 4mW. To reduce standby power in future releases, power-down modes could be used to control high V_t devices in series with the supplies. A second chip fabricated with all high V_t devices has a standby power of less than 50pW, giving some indication of the improvement.

V. PROGRAMMABLE DIGITAL SIGNAL PROCESSORS FOR 4G MOBILE

A. DSP processors for 4G

3G supports multimedia Internet-type services at better speeds and quality compared to 2G. The W-CDMA based air-interface has been designed to provide improved high-capacity coverage for medium bit rates (384kbit/s) and limited coverage at up to 2 Mbit/s (in indoor environments). Statistical multiplexing on the air also improves the efficiency of packet mode transmission. There are certain limitations with 3G as follows higher data rate is difficult with CDMA due to excessive interference between services. It is difficult to provide a full range of multi-rate services, 4G is highly dynamic in terms of support for: the user's traffic, air interfaces and terminal types, radio environments, quality-of-service types and mobility patterns.

4G, puts more demand with adjustable and built-in intelligence. Thus a software system rather than a hard-and-fixed physical system is required. A 4G system is required to provide a comprehensive and secure all-IP based mobile broadband solution to laptop, computer, wireless modems, smart phones and other mobile devices. Facilities such as ultra-broadband Internet access, IP telephony, gaming facilities, may possibly be provided to manipulators. In modern DSP's, architecture can be extended by duplicating the processor cores. Enhanced DSP's utilizes SIMD operations, while multiple-issue DSP's may implement either VLIW or superscalar architectures

System on Chip (SoC) based architectures Mobile device processor architecture became

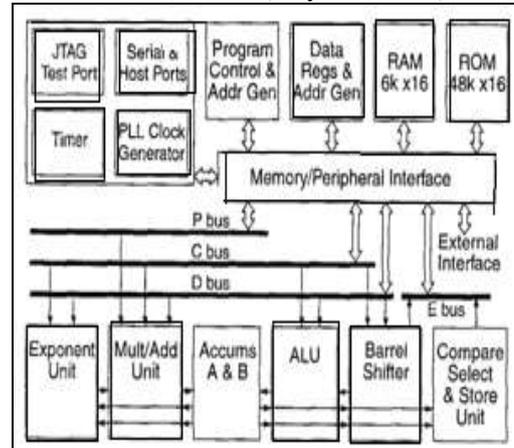


Figure 1: Processor block diagram.

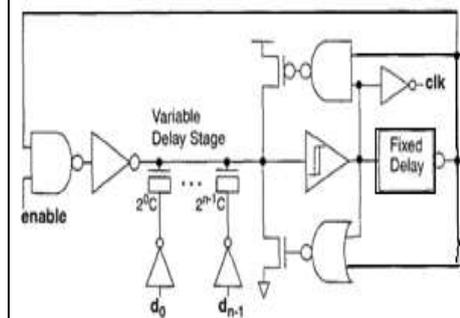


Figure 2: Digitally-controlled oscillator in digital PLL.

Fig. 1 Block diagrams of Modified Harvard Architecture

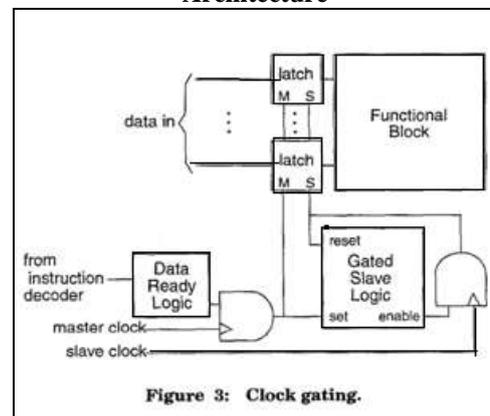


Figure 3: Clock gating.

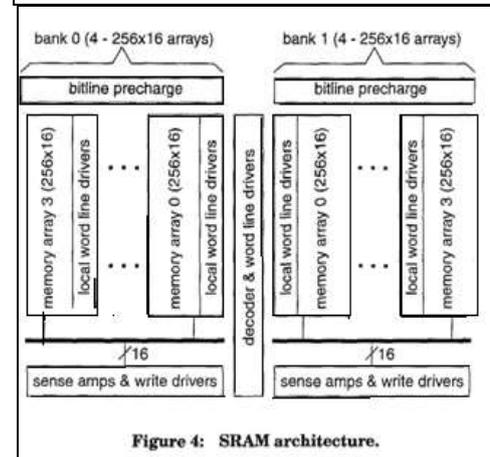


Figure 4: SRAM architecture.

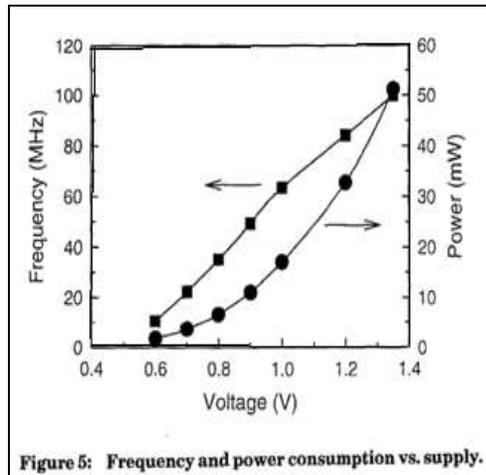


Figure 5: Frequency and power consumption vs. supply.

Simple with SOC designs. Real time responsiveness in mobile devices can be managed by using an improved DSP hybrid chip. dropping the voltage of the chip enables low power operation in mobile devices. Dynamically Configurable System on Chip (CSoC) architecture has been enhanced for mobile communications. CSoC's are modified for a specific application. Its architecture consists of processor core, memory, ASIC cores, and on-chip reconfigurable hardware units. Most of the smart phones are single or dual-core SoC's. For mobile applications, faster dual-core CPU provides better performance than quad-core SoC's. Future SoC's for mobile will become more sophisticated providing better performance.

ARM Processors for Mobiles ARM based processors are the most widely used in modern Smart phones. ARM is a 32-bit instruction set architecture based on RISC architecture [15]. ARM processors are specially used in Smart phones because of its low power consumption and great performance. Different ARM architectures used in Smartphone are ARMv5 used in low-end devices, and ARMv6, ARMv7 used in high performance devices. ARMv7 has a hardware floating-point unit (FPU) providing improved speed. The 32-bit ARM architecture, such as ARMv7-A, is the most extensively used architecture in mobile devices. ARM architecture is the main hardware architecture for many of the operating systems of mobile devices such as iOS, Android, Windows Phone, Windows RT, Bada Blackberry OS/Blackberry10, MeeGo, Firefox OS, Tizen, Ubuntu Touch, Sailfish and Igelle OS.

VI. CONCLUSION

Designers of 3G base stations will make use of the DSPs in order to achieve the high performance and flexibility needed for tomorrow's voice and data applications. Speech coding is an essential application of digital signal processing in modern day telephony and mobile communications, which employ high data compression ratios. Effective embodiment of these design principles will fulfil the promise of 3G to provide the foundations of the kind of wireless infrastructure necessary for tomorrow's applications.

We have discussed that by using Harvard architecture in the cpu will decrease the operating voltage in the mobile,

advanced functionality in mobile devices from the major manufacturers, and with fourth generation (4G) wireless broadband.

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BIOGRAPHY

Mrs. Vasudha Rajesh Gujar received the M.Tech degree in Power Electronics from PDA College of Engineering Gulbarga. She is currently working as a lecturer, from the year 2005 in the Department of Electronics and communications engineering, in Basavakalyan Engineering College at Basavakalyan. Her research interest includes Digital signal processing and Digital signal processing architectures for wireless communications