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NOVEL TECHNIQUES FOR IMPROVEMENTS IN SEQUENTIAL SWITCHING SHUNT REGULATOR FOR SPACECRAFT

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Abstract— **This article presents an improved topology of Sequential Switching Shunt Regulator System to reduce the inherent power loss and the effect of Electro Magnetic Interference (EMI). The non-redundant diode which is used to block the reverse flow current from the Bus capacitance has been replaced by a Synchronous MOSFET. The power loss analysis is done for both the diode topology and also using the MOSFET. A novel hysteresis setting is done to achieve single string switching to reduce the effect of EMI. The experimental results are also presented in this article.**

Index Terms— **Sequntial Switching Shunt Regulator; inherent power loss; non-redundant diode; Synchronous MOSFET;Electro Magnetic Interfernce; Single String Switching;**

I. INTRODUCTION

Power conditioning unit controls the overall power flow in a satellite. Power Regulator is the main component of Spacecraft Power System. It maintains the power bus voltage at a constant level irrespective of the changes in the input or disturbances in load. The key requirements of power regulators are reliability, efficiency, compactness and autonomy with good regulation. Over the years, many topologies are being used for controlling the power supplied to the power bus of a spacecraft. The Sequential Switching Shunt Regulator (S3R) system is one of the standard topologies used in a spacecraft to regulate the power bus voltage at a constant value. The nonredundant diode used to block the reverse flow of current from the power bus when the shunt switch is ON. The use of this diode incurs a power loss thereby reducing the efficiency of the system. If two such diodes are used for redundancy purpose then the power loss will be still higher. To reduce this inherent power loss across the diode, a synchronous MOSFET is used. The noise coupling is reduced by achieving single sting switching. The operation of the S3R is presented in the next section.

II. SEQUENTIAL SWITCHING SHUNT REGULATOR(S3R)

The mechanism of the sequential switching shunt is illustrated in Fig. 1. Optimum number of solar array strings is connected to the load to supply th desied current value. The switches S1, S2, S3, connect the solar array strings to either load or shunts away depending on the load requirement. The diodes D1, D2, D3 avoid the short circuit of the bus capacitance when the shunt switches are ON.

During the initial stage (power on), the bus voltage is zero. Therefore all the switches are open to supply the sufficient current to charge the bus capacitance. As the bus voltage rises, the switches close sequentially till the voltage reaches the desired value.

If all the switches close then there will be insufficient current to the bus then the last switch opens to supply the current. In this way the switches open sequentially till the desired voltage level is reached by the load. The bus voltage is maintained between the two levels set by the Schmitt triggers C1, C2, Cn as shown

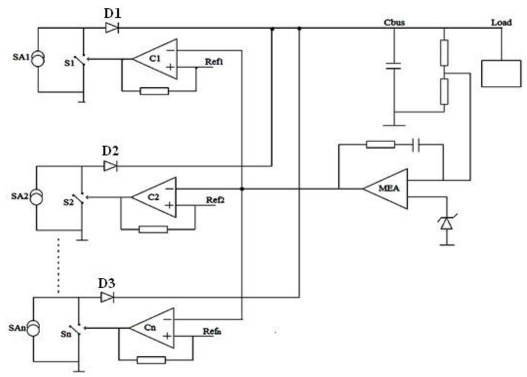

Fig. 1 S3R Mechanism

If any one of the diodes D1, D2, Dn, fails (short circuited), then the entire system gets collapsed. In Space applications a single point failure should not affect the functionality of the entire system. So to bring in redundancy two such diodes are used in series. But this increases the inherent power loss. So a novel topology of shunt regulator using the synchronous switching is presented in this article.

III. SYNCHRONOUS SWITCHING

A novel technique of synchronous switching is implemented as shown in Fig. 2. The diode has been replaced by a MOSFET Q2 as shown in the figure.

Here the MOSFET Q2 is not connected in the conventional way. The source is connected to the Solar Array side and the drain is connected to the load side. This is because the internal body diode present should not short the power bus when the shunt MOSFET switch Q1 is on.

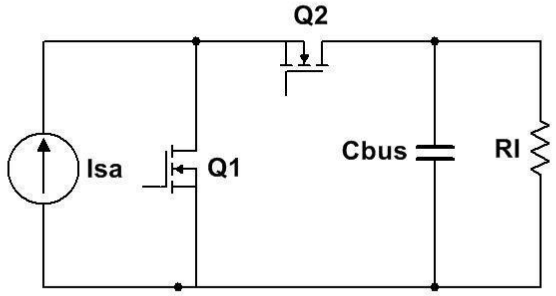

Fig. 2 Sunchronous Switching to reduce the inherent power loss.

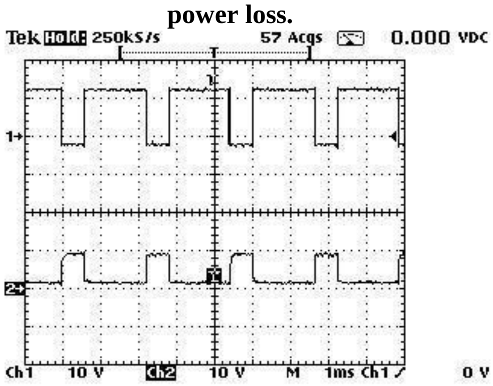

Fig.3 Gating signals for the Synchronous Switching

An opto-coupler and a transistor inverter are used to generate the gating signals for the switch Q2. The gating signals generated are shown in Fig.3. The first signal is for the switch Q2 which is generated from the second signal which is to drive the switch Q1. The opto-coupler and transistor based gate drive for switch Q2 is given in Fig.4

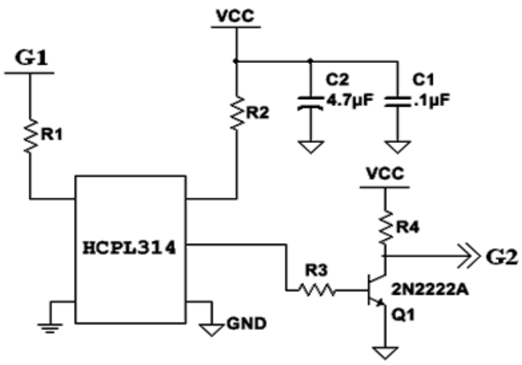

Fig. 4. Opto-coupler based gate drive.

The waveforms in Fig. 5 and Fig. 6 show the voltage and current of the non-redundant diode. The waveforms are taken for the maximum rise time of 10us. The power loss across the diode is calculated using these waveforms.

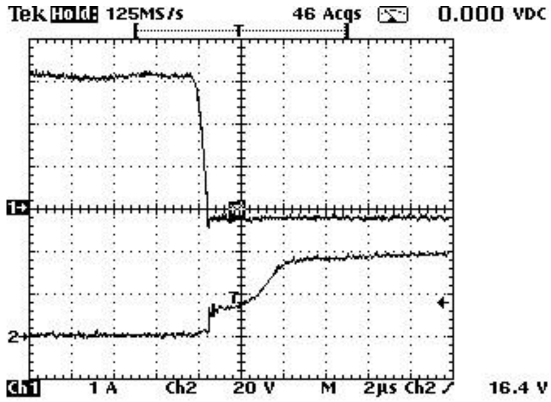

Fig. 5 Diode Current fall and voltage rise

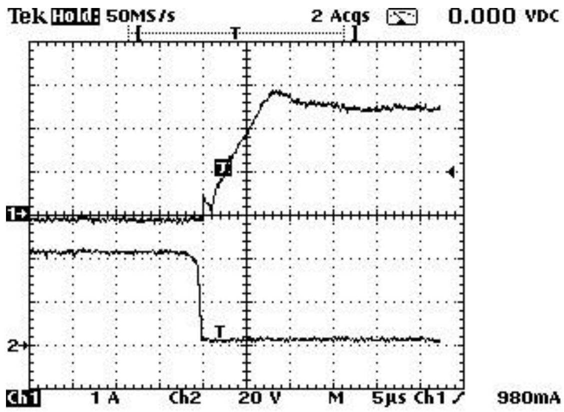

Fig. 6 Diode Current rise and voltage fall

The Fig. 7 and Fig. 8 show the voltage and current waveforms of the Synchronous MOSFET. The waveforms are taken for the maximum rise time of 10us. The power loss across the MOSFET is calculated using these waveforms.

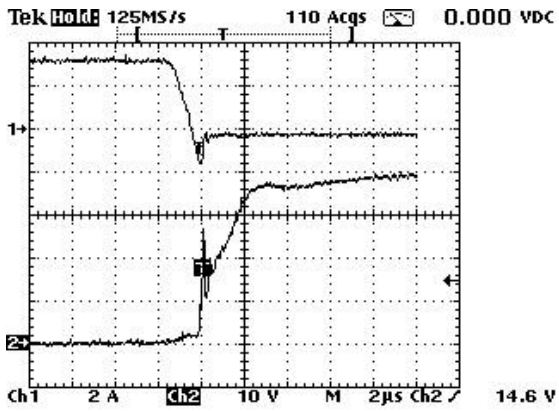

Fig. 7 MOSFET Current fall and voltage rise

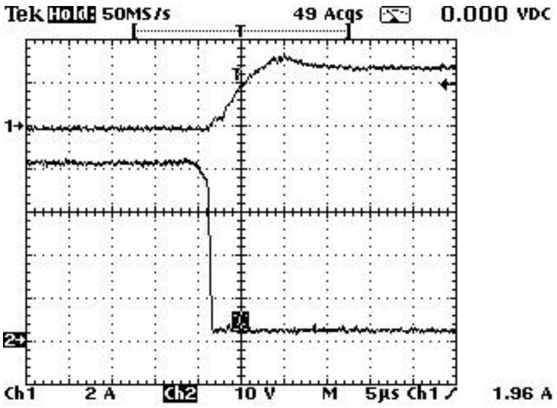

Fig. 8 MOSFET Current rise and voltage fall

The power loss comparison between diode and MOSFET is given in Table 1. The power loss for the MOSFET is calculated for the maximum rise time of 10us. From the table it is clear that the power loss across the MOSFET is very less compared to the power loss across the diode. Even if two MOSFETs are incorporated for the redundancy, still the power loss will be less compared to the diode.

Table I. POWER LOSS COMPARISON

Switch Type	Power Loss (W)	Reduction (%)
Diode	5.1096	51.36
MOSFET	2.485	

IV. Single String switching

The conventional way of hysteresis setting allows all the string to be switching depending on the load condition. The noise coupling with the neighboring circuit is more in this case. A novel technique of hysteresis setting is proposed to reduce the noise generated. The current and the proposed hysteresis techniques are shown in Fig. 9 and Fig. 10.

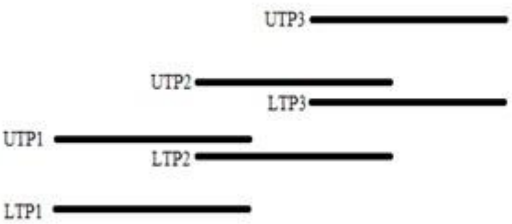

Fig. 9 Present hysteresis levels

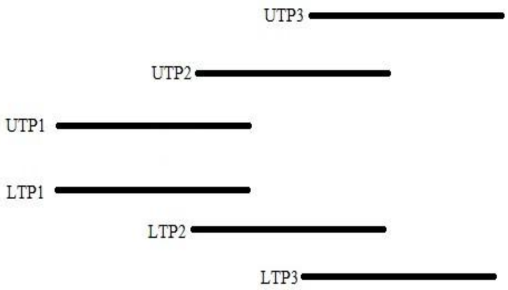

Fig.10. Proposed hysteresis levels

The smallest hysteresis level dictates the bus ripple. The levels of hysteresis comparator for the new technique (Figure 10) is given,

LTP1=1V LTP2=0.5V LTP3= 0V
UTP1=2V UTP2=2.5V UTP3=3V

The advantage offered by the introduced topology is that only one MOSFET experiences switching whereas the others are either shunt or open. So if the switching string is shielded then the noise coupling with the neighboring circuit drastically reduces.

The gating signals generated with the new hysteresis levels for the different load conditions are shown in Figure 11, 12 and 13.

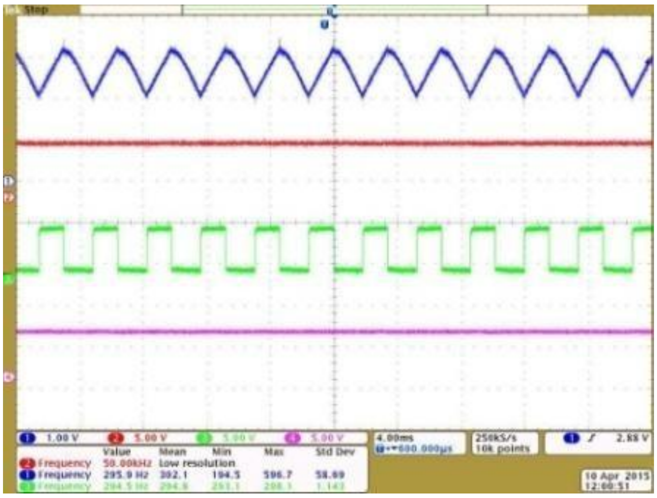

Fig.11.Minimum Load Condition

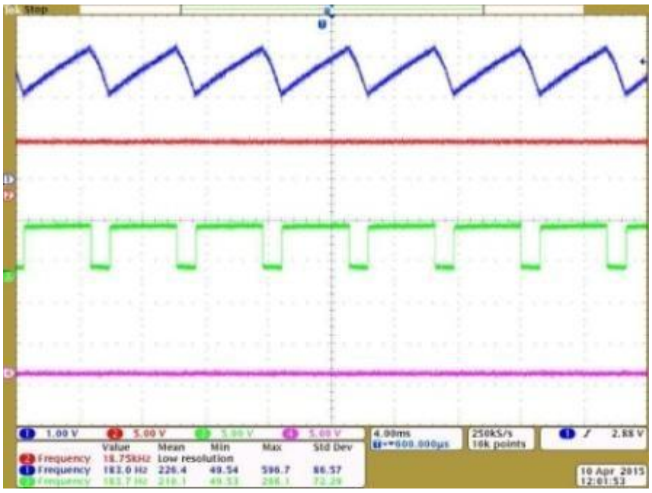

Fig.12.Medium Load Condition

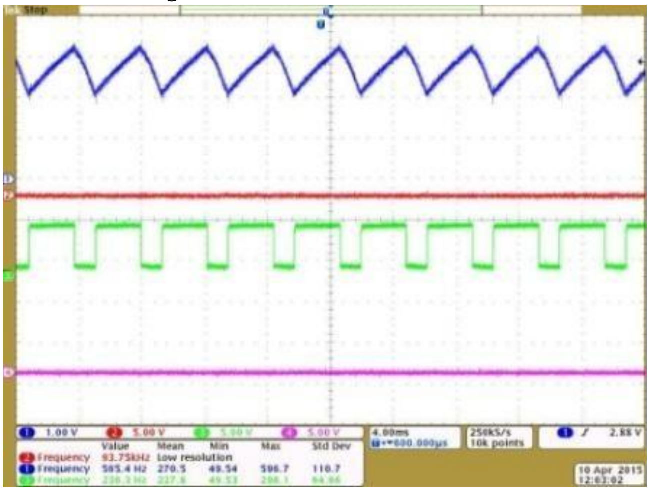

Fig.13.Maximum Load Condition

It is clear that at any load condition only one string is switching. The same string switches for all load conditions and if that string is shielded then the noise coupling with the neighboring reduces drastically.

V. CONCLUSION

The Sequential Switching Shunt Regulator System is uses in the geosynchronous and the geostationary satellites of the Indian Space Program. The improved topology presented in this article reduces the power dissipation to a great extent which is one of the major requirements of any spacecraft power system. The novel technique of hysteresis setting to achieve single sting switching reduces the noise coupling drastically.

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