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DESIGN AND PERFORMANCE ANALYSIS OF LOW POWER TWO STAGE OP-AMP

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***Abstract*— A Low power CMOS operational amplifier (Op-Amp) which operates at 1.8V power supply. The unique behavior of the MOS transistors in saturation region not only allows a designer to work at a low voltage, but also at a high frequency. Designing of two-stage op-amps is a multi-dimensional optimization problem where optimization of one or more parameters may easily result into degradation of others. The Op-Amp is designed to exhibit a unity gain frequency of 20MHz and exhibits a gain of 68.24dB. The ability adopted, to use smaller compensation capacitor (CC), which improves the slew rate and also, benefits for the area of compensation circuit. In order to verify the viability two-stage op-amp at SCNO 180 nm CMOS technology. Power consumption is reducing.**

***Index Terms*— OP-AMP, CMOS, Compensation Capacitor, Optimisation.**

I. INTRODUCTION

CMOS op amps are ubiquitous integral parts in various analog and mixed-signal circuits. The term OTA was originally conceived for operational trans conductance amplifiers with linear trans conductance (used for the implementation of continuous-time filters), for the sake of simplicity we will use the same term OTA for general operational trans conductance amplifiers. The two-stage Op-Amp shown in Fig. 1 is widely used because of its simple structure and robustness. In designing an op-amp, numerous electrical characteristics, e.g., gain-bandwidth, phase margin common-mode range, offset, all have to be taken into consideration. Furthermore, since op-amps are designed to be operated with negative-feedback connection, frequency compensation is necessary for closed-loop stability. Unfortunately, in order to achieve the required degree of stability, generally indicated by phase margin, other performance parameters are usually compromised. As a result, designing an op-amp that meets all specifications needs a good compensation strategy and design methodology.

Designing high-performance analog integrated circuits is becoming increasingly exigent with the flexible trend toward reduced supply voltages. At large supply voltages, there is a tradeoff among various performance parameters. Speed and accuracy are two most important properties of analog circuits, however optimizing circuits for both aspects leads to contradictory demands. The realization of a CMOS OPAMP that combines a considerable dc gain with high unity gain frequency has been a difficult problem. There have been several circuit approaches to evade this problem. The simulation results have been obtained using 180nm SCNO MOSIS Design has been carried out in Cadence virtuoso. Simulation results are verified.

II. PROPOSED METHOD

The basic equations and parameters are described below. These design main parameters are: phase margin *(*M_Φ*)*, gain-bandwidth product *(*f_{GBW}*)*, load capacitance *(*C_L*)*, slew rate (*SR*), input common mode range (I*CMR*), in this circuit replacing the current source and uses PMOS active load.
Using formula in current and resister and accepted ratio

$$R= 1/K'S(V_{GS}-V_T) \quad (1)$$

Where S=W/L

$K'=\mu_0 C_{OX}$

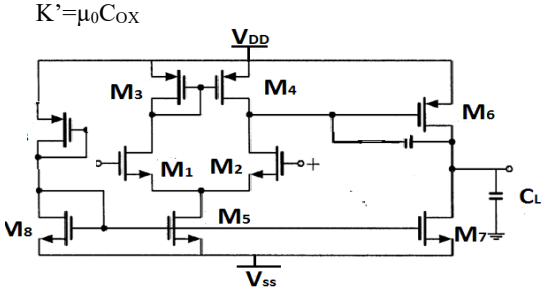

Figure 1. Two stage op-amp

The equations for determining the various Op-Amp characteristics can be shown as follows:

A. Gain and Bandwidth

According to the equivalent circuit shown in Figure 2 under typical conditions
The dc gain of op-amp is given by

$$A=20 \log V0/VIN \quad (2)$$

By placing differential pair M1, M2, M3,M4. It is possible to obtain rail to rail input stage.

B. Common Mode range

If we define V_{CM} as the op-amp input common Mode range i.e

$$V_{CM}^{+} = V_{DD} - V_{CM}(max) \quad (3)$$

And

$$V_{CM}^{-} = V_{CM}(min) - V_{SS} \quad (4)$$

C. Internal Slew Rate

The slew rate associated with C_C is found to be

$$SR = \frac{I_{D5}}{C_C} \quad (5)$$

D. External Slew Rate

The slew rate associated with C_L is found to be

$$SR = \frac{I_{D7} - I_{D5}}{C_L} \quad (6)$$

Combining both above equations we obtain

$$I_{D7} = SR(C_C + C_L) \quad (7)$$

DESIGN STEPS FOR TWO-STAGE OP-AMP

In this work, an Op-Amp has been designed which exhibits high unity gain frequency for optimized balancing of phase margin, gain, power, and load. A method is proposed to set a higher unity gain frequency of the Op-Amp working at a lower supply voltage. This allows the value of each circuit element of the amplifier (i.e. transistor aspect ratios, bias current and compensation capacitor) to be univocally related to the required electrical parameters.

Here we have chosen a simple differential pair amplifier for input amplifier, common source amplifier (high gain, swing balancing) for output amplifier, a current mirror circuit and a biasing circuit, and connecting PMOS load in input (replacing current source) with a Miller capacitance in series with each other. We see that simulate in above circuit and get DC Gain 54db and GBW 18.15 MH_Z. Then we connected same W/L ratio in series PMOS and NMOS IN Load.

A design steps for two-stage op-amp in Figure 3 can be constructed as follows.

Step1- we have-

$$C_C = \frac{4KT}{3\omega_u k_n (V_{GS1} - V_{TH})} \left[1 + \frac{SR}{\omega_u (V_{GS1} - V_{TH})}\right] \quad (8)$$

Step2-I_{D7} is given as-

$$I_{D7} = SR(C_C + C_L) \quad (9)$$

Step-3 The value of L_6 is given by-

$$L_6 = \sqrt{\frac{8}{2} \frac{k_p V_{DS6}^{sat} C_C}{\omega_u (C_C + C_L) \tan(\Phi_M)}} \quad (10)$$

Step-4 $(W)_6$ is given as-

$$W_6 = \frac{2SR(C_C + C_L)}{k_p C_{ox} (V_{GS6}^{sat})^2} L_6$$

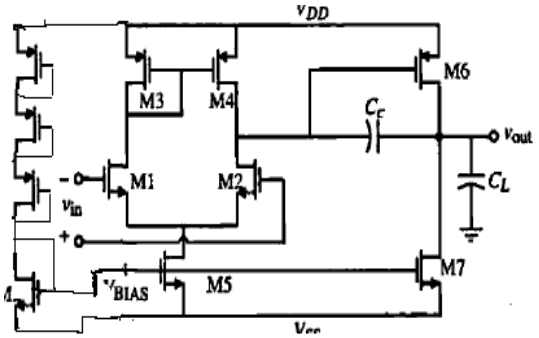

Figure.2. High Frequency Small-Signal Equivalent circuit

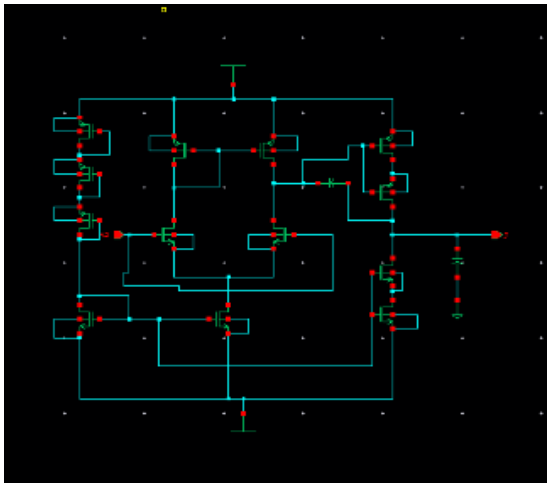

Figure.3 The proposed CMOS Op-Amp circuit

Step-5 I_{D5} is given by

$$I_{D5} = C_C SR \quad (11)$$

Step-6 $(W/L)_{1,2}$ is given as-

$$\left(\frac{W}{L}\right)_{1,2} = \frac{\omega_u^2 C_C}{k_n C_{ox} SR} \quad (12)$$

Step-7 The value of $\left(\frac{W}{L}\right)_{3,4}$ is given by-

$$\left(\frac{W}{L}\right)_{3,4} = \frac{2SRC_C}{k_n C_{ox} \left(V_{GS1,2} - V_{TH} - \frac{SR}{\omega_u}\right)^2} \quad (13)$$

Step-8 Calculate $(W/L)_7$ from the basic relation $(I_{D7}/I_{D5}) = ((W/L)_7/(W/L)_5)$ yields

$$\left(\frac{W}{L}\right)_7 = \left(\frac{C_C + C_L}{C_C}\right)\left(\frac{W}{L}\right)_{3,4} \quad (14)$$

Step-9 $(W/L)_{3,4}$ is given by

$$\left(\frac{W}{L}\right)_{3,4} = \frac{\left(\frac{W}{L}\right)_6}{2\left(\frac{W}{L}\right)_7}\left(\frac{W}{L}\right)_{5,8} \quad (15)$$

Step-10 Using equation 3.22, 3.3, 3.14 and the triode equation we the find value of R_c as-

$$R_c = \frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_7 V_{eff7}} \quad (16)$$

Where $V_{eff7} = V_{DD} - V_{thn}^{max} - 2|V_{tp}|$

So $(W/L)_9$ is given as-

$$(W/L)9 = \frac{2g_{m1,2}}{\mu_p C_{ox} V_{thn}^{max}(V_{DD} - V_{thn}^{max} - 2|V_{tp}|)} \quad (17)$$

III. SIMULATION RESULT

Based on the proposed circuit in Figure.3 Op-Amp has been designed 180nm CMOS technology. The Op-amp is currently being fabricated in SCNO. So only the post simulation results will be presented here.Fig.4 presents the simulated results of for Vdd=1.8V. The process parameter and the electrical specification of CMOS op-amp for 180 nm CMOS technology are tabulated in the Table I and Table II respectively.

Table 1
ELECTRICAL SPECIFICATION OF CMOS Op-Amp

Load capacitance: C_L (pF)	10
Miller compensation capacitances: C_C (pF)	3
Supply voltage	+1.8 V

Table 2
PROCESS PARAMETERS (SCNO180 nm Tech.)

$\mu C_{ox}/2$: NMOS (A/V^2)	173.9
$\mu C_{ox}/2$: PMOS (A/V^2)	35.0
V_{thpmin} (volt)	0.37
V_{thnmax}(volt) NMOS	0.50
ICMR(Volt)	1.3
Vdd(volt)	1.8

Table 3
TWO STAGE OP-AMP DEVICE SIZE

S=W/L	W/L(nm)
S1	540
S2	540
S3	540
S4	540
S5	4.5u
S6	4.5u
S7	1.26u
S8	1.26u
S9	17.82u
S10	30u
S11	8.62u
S12	8.62u
S13	8.62u

A. AC RESPONSE:

Through AC response we can simulate the schematic to find out the bode plot and phase plot.

In Figure 4, a bode plot and phase plot for 1.8 V, 27° C and CL = 10 pf is shown. As can be seen, the open loop gain is 62.05 dB, and a phase margin is -13.69°. The unity gain bandwidth is 17.15 MHz and f bandwidth is 1.74 KHz.

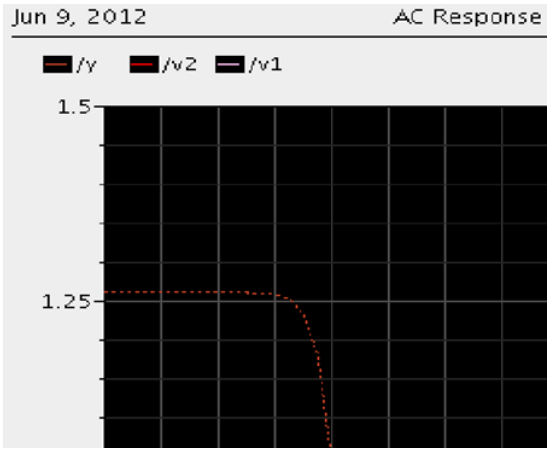

Figure 4.Frequency Response Plot with CL=10 pf

B. TRANSIENT STEP RESPONSE

In Figure 5, a step from ground to VDD is applied at the input with unity feedback configuration.

The slew rate of op-amp is 11.22 V/µS for rising edge of pulse and 11.10 V/ µS for falling edge of the pulse.

Figure 5.Transient Pulse Response of Op-Amp for

C. GAIN AND PHASE:

Fig-6 and Fig-7 shows DC gain and phase. Its represent DC gain is 62db and phase 179 deg at Vdd=1.8 and SCNO 180nm tech.

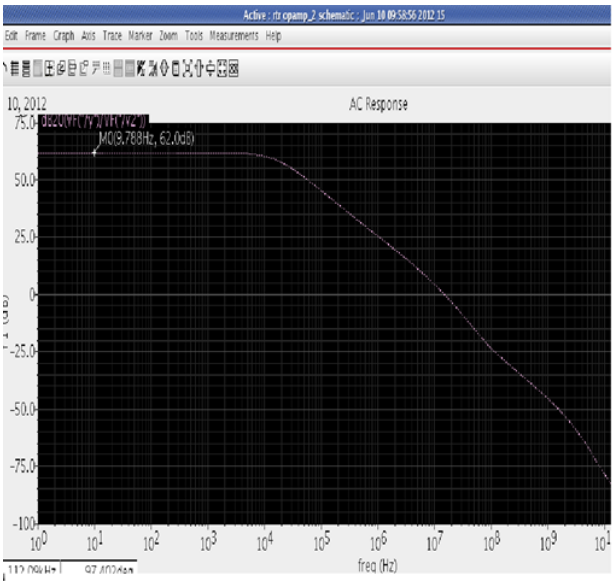

Figure 6 .DC Gain of Op-Amp

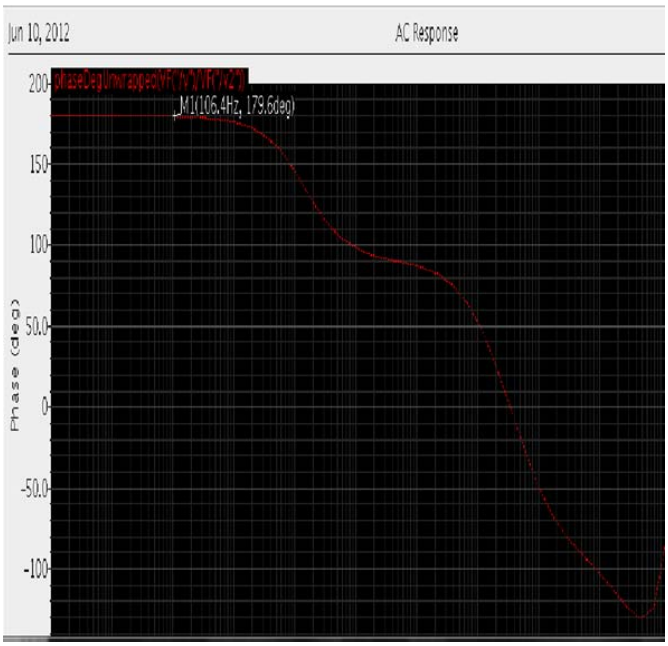

Figure 7. Phase of Op-Amp

D. PHASE AND GAIN MARGIN:

Fig 8 shows that phase margin is 13.69 deg and gain margin is 28.36db after simulation in applied voltage 1.8 and gain 62db and phase 179deg.

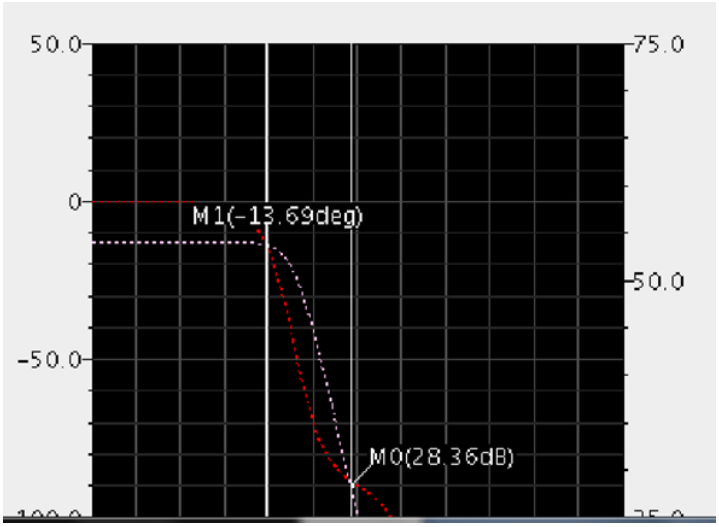

Figure 8 .phase and gain margin of Op-Amp

Table 4
Simulation Results of Op-Amp (180nm Technology)

Specifications	Theoretically value	Simulation results
DC gain (dB)	**54**	68.24
GB (MHz)	20	19.3
Phase margin	-	-15.69
CMRR (dB)	**-158.2**	89.67
ICMR (V)	1.3	0.9
Slew rate (V/µS)	10.8	12.2
Power dissipation(µW)	109.4	-
I_{D5}(µA)	32.4	35.78
I_{D8}(µA)	32.4	37.78
Load capacitance (pf)	10	10
Supply voltage (V)	1.8	1.8

IV. TEST AND MEASUREMENT

To determine the dc gain improvement provide by the introduce structure. We have realized two stages Op-Amp in 180 nm CMOS technology. In the figures 5 we have simulate it to calculate the transient response, fig-6 shows DC gain, fig-7 phase and fig 8 shows gain margin and phase margin in table 3 we simulate the proposed Op-Amp at 180 nm and measure the performance. By the proposed structure we got excellent result of dc gain and Slew rate. If it is less than the simulated one (not totally realistic, because technology dispersion is not taken into account) dc gain and GBW shows increase DC gain decrease GBW frequency. Then I say that yet increase bandwidth of op-amp then balance DC Gain, good being to amplifier. If increase frequency then these amplifier work at oscillator .so we have to balance condition in both. We do not have yet the simulation result for the Op-Amp realized at 180 nm with 1.8 V V_{DD}.

V. CONCLUSION

We simulate the proposed Op-Amp at 180 nm using cadence virtuous and measure the performance. By the proposed structure we got excellent result of dc gain and Slew rate. If it is less than the simulated one (not totally realistic, because technology dispersion is not taken into account) dc gain and GBW shows increase DC gain decrease GBW frequency. Then I say that yet increase bandwidth of op-amp then balance DC Gain, good being to amplifier. if increase frequency then these amplifier work at oscillator .so we have to balance condition in both

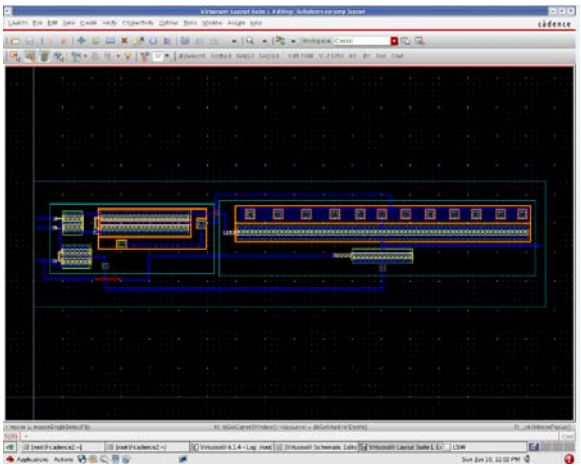

Figure 9 Layout of proposed op-amp circuit

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