International Journal of Technical Research and Applications e-ISSN: 2320-8163,
www.ijtra.com Special Issue 31(September, 2015), PP. 231-233

DESIGN OF CMOS INVERTER USING LECTOR TECHNIQUE TO REDUCE THE LEAKAGE POWER

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Abstract: **The scaling down of CMOS circuits has resulted in increasing the sub-threshold leakage current with the decrease in the threshold voltage. LECTOR is a method to decrease the problem of leakage in CMOS circuits, it includes two extra leakage control transistors, which are self-controlled, in the pathway from supply to ground which offers the extra resistance which will reduce the problem of leakage current in the CMOS circuit. This paper concentrates on the analysis of leakage current in basic CMOS Inverter employing LECTOR technique using Cadence 45nm technology.**

Key words: **leakage current, Sub-Threshold leakage, DIBL, Body bias, LECTOR.**

I. INTRODUCTION

In last few decades, much attention has been given to low power integrated circuit design because the power consumption is an important aspect in VLSI circuits. The modern electronics industry is witnessing for miniaturization in every corners of electronics and communications in the field of wireless communication, bio-medical application, computers, processors etc. Designing and developing highly efficient analog circuits is becoming a challenging task along with the reduction in supply voltage. An important factor pertaining to analog circuit is, the threshold voltages of CMOS technologies are not guaranteed to decrease much below than which is available these days. Due to increase in power consumption of present day chips, the pioneering cooling and packing policies are of little help and the burden associated with the packing and cooling of such CMOS devices is a challenging task. In accumulation to cost, the reliability problem is a major aspect in CMOS circuits. With the doubling of on chip transistors in every two years, minimizing the power consumption has become currently a challenging area of research [1], [2].

II. POWER DISSIPATION IN CMOS

Power dissipation is arisen as a significant constraint in the microelectronic circuits designing, exclusively in gadgets, computing elements and wireless mobile applications [1], [2], [3].

This paper deal with reduction and optimization techniques for leakage power dissipation in CMOS circuits. The causes of power dissipation in CMOS circuits are described by the equation (1).

$$P=1/2.C.V_{DD}^2.\ f.\ N + I_{leak}\ .V_{DD} + Q_{SC}\ .VDD.\ f\ .N \qquad (1)$$

Where P signifies the total power dissipated, V_{DD} represents the supply voltage, and f represents the operating frequency. The first term denotes the power required for charging and discharging the circuit nodes. Capacitance of the node is C. The factor N is the switching action which gives the number of gate transitions per clock cycle at the output. The second term in Equation 1 signifies the static power dissipation due to the leakage current I_{leak}. The third term in Equation 1 signifies power dissipation when output change overs owing to short-circuit current flowing from the supply V_{DD} to ground. The term Q_{SC} symbolises the amount of charge carried during each transition by the short circuit current in the circuit.

III. SUBTHRESHOLD LEAKAGE

The sub threshold current in the MOSFET is the source to drain current of the MOSFET in weak inversion mode [2], [4]. The parameters that disturb the threshold voltage and the leakage current in the circuits are as follows:

A. Drain-Induced Barrier Lowering (DIBL):

A MOSFET is said to be a short channel device when the length of the channel is of the order of the depletion width of the source/drain junction. When gate voltage in long channel device is adequately lesser than the threshold voltage, electrons from the source region are prohibited to inflowing into channel owing to generation of potential barrier at the source to channel junction. But, in case of short-channel devices, this barrier is dropped by the drain electric field, which ultimately permits the electrons to drift into the channel. This drift of electrons

increases the drain current, which further increases the sub-threshold leakage current and also the static leakage power. In short channel devices, DIBL consequence is well-ordered by increasing the channel doping, but such improved doping will reduce the carrier mobility and hereafter the drain current.

B. Effect of body bias

The expression (2) of threshold voltage for substrate bias is characteristic as:

$$VT(VSB) = VTO + \gamma [(|2\phi F| + VSB)^{1/2} - (|2\phi F|)^{1/2}] \quad (2)$$

Where, VT (VSB) is the substrate-bias at zero threshold voltage, γ is the substrate bias coefficient (usually equal to 0.4V-0.5V) , ¢*F* is the Fermi potential; *VSB* is the substrate bias potential.
Due to decrease in supply voltage and body bias, leakage current of the circuit also losses along with the threshold voltage.

C. Effect of temperature

The threshold voltage also depends on the temperature which affects the sub-threshold leakage current. Threshold voltage has the temperature sensitivity of 8mV/ ºC.

IV. LECTOR TECHNIQUE

For reduction in the leakage power, the assembling of transistors from V_{DD} to ground is the notion behind the LECTOR technique [3], [5]. In this method, two leakage control transistors are positioned in between the pull-up and pull-down network, this implies either one of the LCTs will continuously drives in its near cut-off region, this arrangement is shown below in Figure 1.

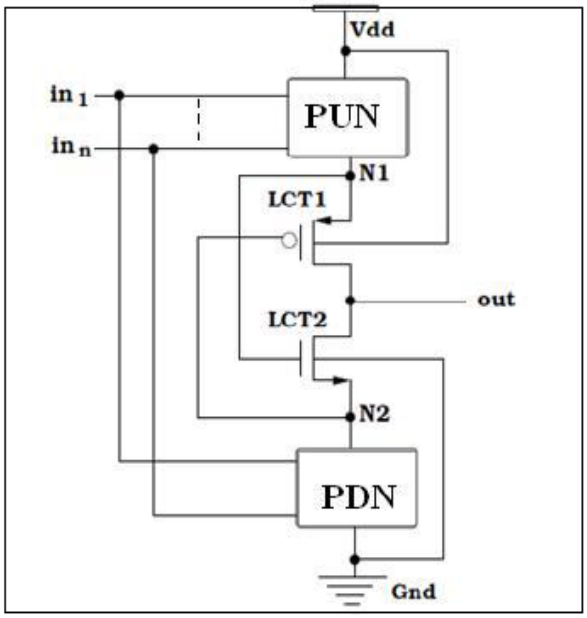

Figure 1: LECTOR CMOS Gate.

Between two nodes N1 and N2, LCT's are introduced. The gate of the LCT's is controlled by the source of the other. Since LCTs are self-controlled there is no need of external circuit. These two LCTs increases the resistance between V_{DD} and ground, and thereby shrink the leakage current. The CMOS inverter without and with LECTOR is shown in Figure 2 and Figure 3 respectively

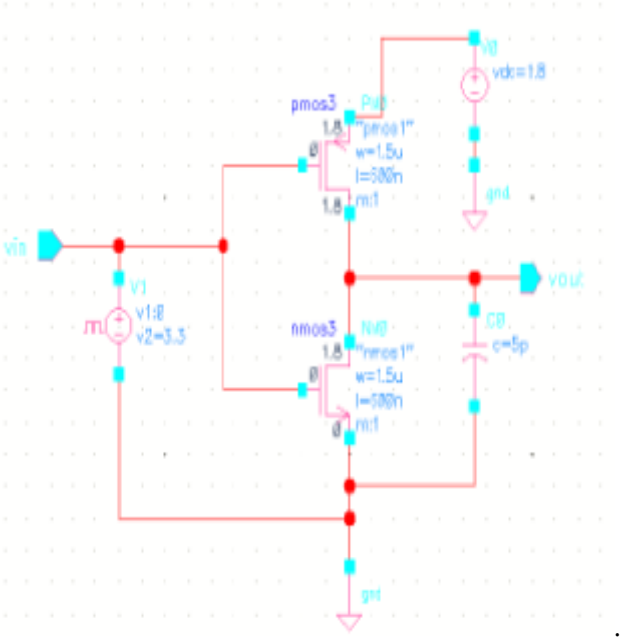

Figure 2: CMOS inverter without LECTOR.

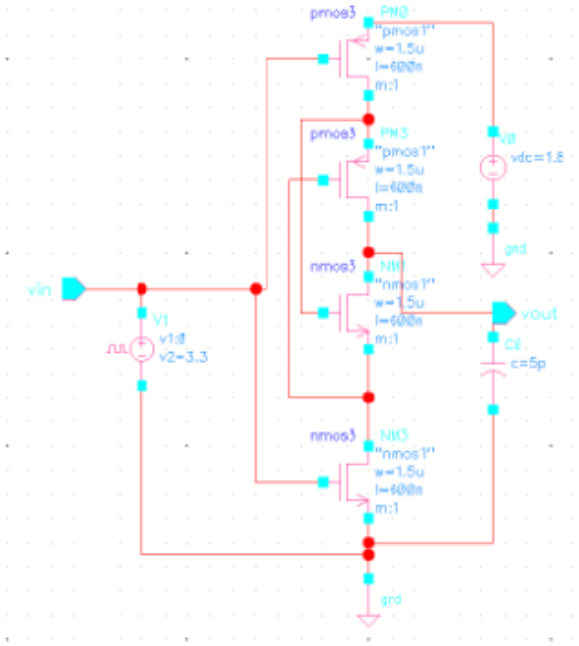

Figure 3: CMOS Inverter with LECTOR

The simulation waveform for CMOS inverter with and without LECTOR is shown in the Figure 4 and Figure 5 respectively.

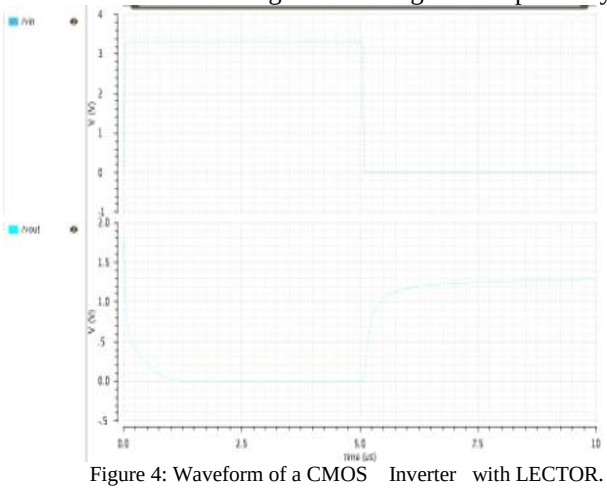

Figure 4: Waveform of a CMOS Inverter with LECTOR.

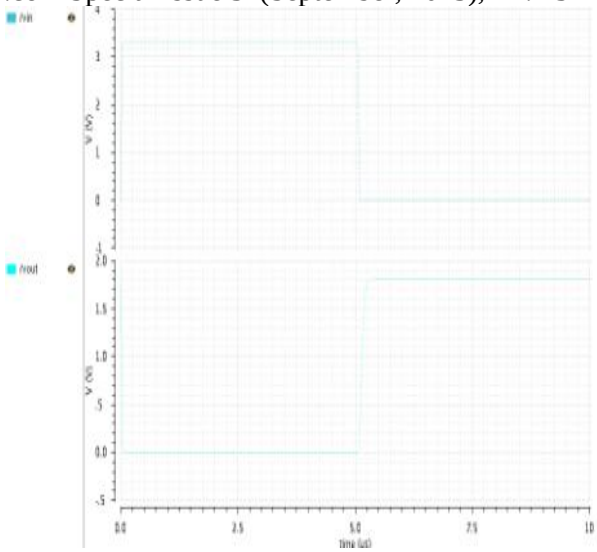

Figure 5: Waveform of a CMOS Inverter without LECTOR.

V. CONCLUSION

Using cadence at 180nm CMOS technology total power consumed by the CMOS inverter without LECTOR with a load capacitor of 5pF is about1.632E-6.and with LECTOR is 1.168E-6 If we hand calculated the dynamic power dissipation for this device using the formula for dynamic power: $P_{dyn} = C_L * V_{DD}^2 *$ frequency= 5pF * 1.8^2* (1/10us) = 1.62 * 10^{-6}, we see that the result obtained from theoretical (formula) calculation isn't too far off from our simulation result.

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