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IMPLEMENTATION OF NEURAL NETWORK FOR SIGNAL COMPRESSION AND DECOMPRESSION USING 45 NM CMOS TCHNOLOGY

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Abstract— **The advancement in medical science we are trying to process the information artificially since our biological system performs inside our body. Artificial intelligence through a biological word is realized based on mathematical equations and artificial neurons. Our main focus is on the implementation of Neural Network Architecture (NNA) with on chip learning in analog VLSI for generic signal processing applications. In the proposed paper analog components like Gilbert Cell Multiplier (GCM), Neuron activation Function (NAF) are used to implement artificial NNA. The analog components used are comprises of multipliers and adders' along with the tan-sigmoid function circuit using MOS transistor in sub threshold region. This neural architecture is trained using Back propagation (BP) algorithm in analog domain with new techniques of weight storage. Layout design and verification of the proposed design is carried out using micriwind3.1 software tool. The technology used in designing the layout is 45nm CMOS technology**

Index Terms **Neural Network Architecture, Gilbert cell Multiplier, Neuron activation Function, Back Propagation Algorithm.**

I. INTRODUCTION

A. Artificial Intelligence

The intelligence is a biological word and is acquired from past experiences. The science which defines intelligence mathematically is called as Artificial Intelligence (AI). Artificial neurons is used for implementing the Artificial Intelligence as Artificial & it has comprised of several analog components. Intelligence is the computational part of the ability to achieve goals in the world. The proposed of this paper is the implementation of neural network architecture using back propagation algorithm for data compression & decompression. The neuron selected by comprises of multiplier and adder along with the tan-sigmoid function. The training algorithm used is performed in analog domain because of this the whole neural architecture is an analog structure.

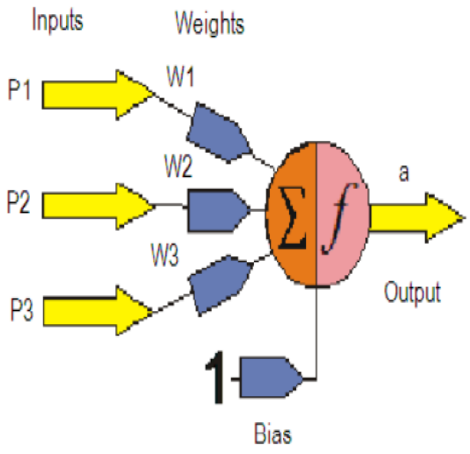

Figure 1: Neural Network

Figure 1 can be expressed mathematically as

a = f (P1W1+P2W2+P3W3+Bias)

where „a_ is the output of the neuron & „p_ is input and „w_ is neuron weight . The bias is optional and user defined. A neuron in a network is a simple processing unit & its input has asociated with weight. Weight are used to increases the strength of the input signal and produces an output. The working of neuron is to add together all the inputs and calculating an output to be passed on. To train the neural Architecture we can used the back propagation algorithm and it is also feed forward network.

The designed neuron is suitable for both analog as well as digital applications, but we used the analog application which performing operation like sine wave learning, amplification and Frequency multiplication and can also be used for analog signal processing activities.

B. Multiple Layers of Neurons

The multiple layers of Neurons is set of single layer neurons are connected with each other as shown in the figure 2.

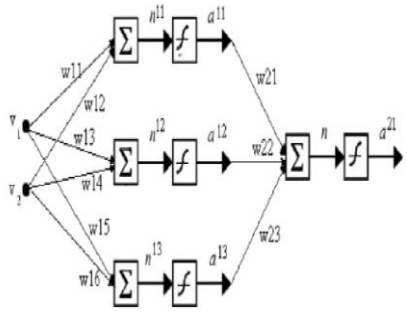

Figure 2: Layered structure of Neural Network

From the above figure it is clear that weights w11 to w16 are used to connect the inputs v1 and v2 to the neuron in the hidden layer. Then weights w21 to w23 transferred the output of hidden layer to the output layer. The final output is a21.

II. .SYSTEM ARCHITECTURE :

A. Analog Components for Neural Architecture

The input v1 and v2 of neuron has multiplied with weight matrix, the output is summed up and is passed through an NAF. The output of the activation function is then passes to the next layer for further processing. Blocks to be used are Multiplier block, Adders, NAF block with derivative.

B. Multiplier Block

The Gilbert cell is used as the multiplier block. The schematic of the Gilbert cell is as shown in the figure 3.

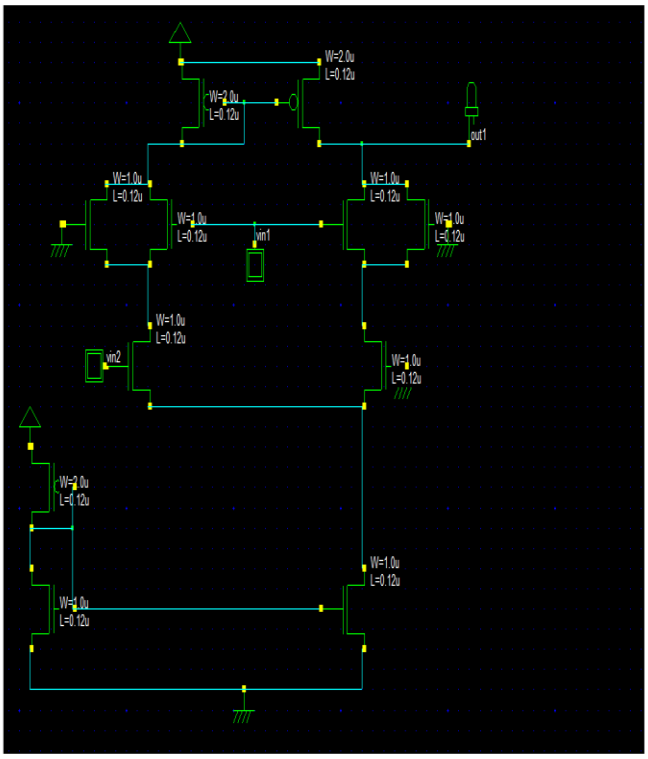

Figure 3: Gilbert cell schematic with current mirror circuit

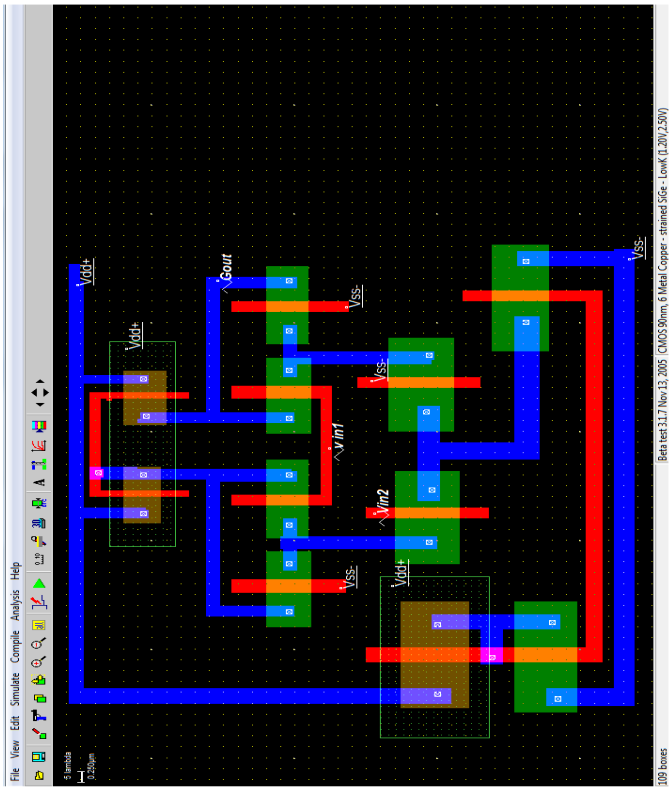

Figure 4: Layout of Gilbert cell multiplier

As in this paper we are mainly focusing on layout part so the layout of the Gilbert cell multiplier is shown in figure 4. Layout design and verification of the proposed design is carried out using microwind3.1 software tool. The technology used in designing the layouts is 45nm CMOS technology.

C. Adders

The output of the Gilbert cell is in the form of current (trans conductance).The node of the Gilbert cell is connecting the respective outputs nothing but the adder itself.

D. Neuron Activation Function (NAF)

The designed activation function is tan sigmoid. The design of the NAF is actually a differential Amplifier which has modified for differential output. Same circuit is capable for producing differentiation output of the activation function. Here two designs are considered for NAF ,

a. Differential amplifier as NAF
b. Modified differential amplifier as NAF with differentiation output.

a. Differential Amplifier Design as A Neuron Activation Function (Tan)

This block is named as tan in the final schematics for Neural Architecture. Differential amplifier when design to work in the sub-threshold region acts as a neuron activation function.

b. Modified Differential Amplifier Design for Differentiation Output (fun)

Schematic of the design shown in the figure 5 is used for the tan sigmoid function generator with modification for the differential output. The NAF function can be derived from the same differential pair configuration. The structure has to be modified for the differential output.

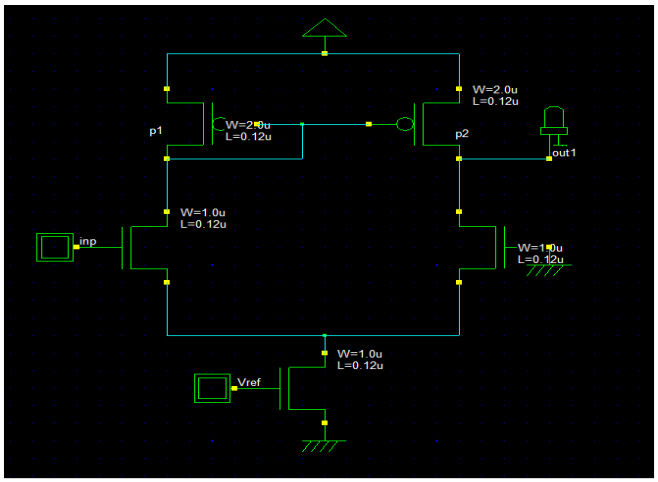

Figure 5: Schematic of NAF

E. Layout issues

We are using tan sigmoid function to realize NAF because by using tan- sigmoid function is that after carried out a mathematical analysis we found that tan sigmoid function is best suitable for compression and achieving a tangential output. The layout of NAF is shown in figure 6.

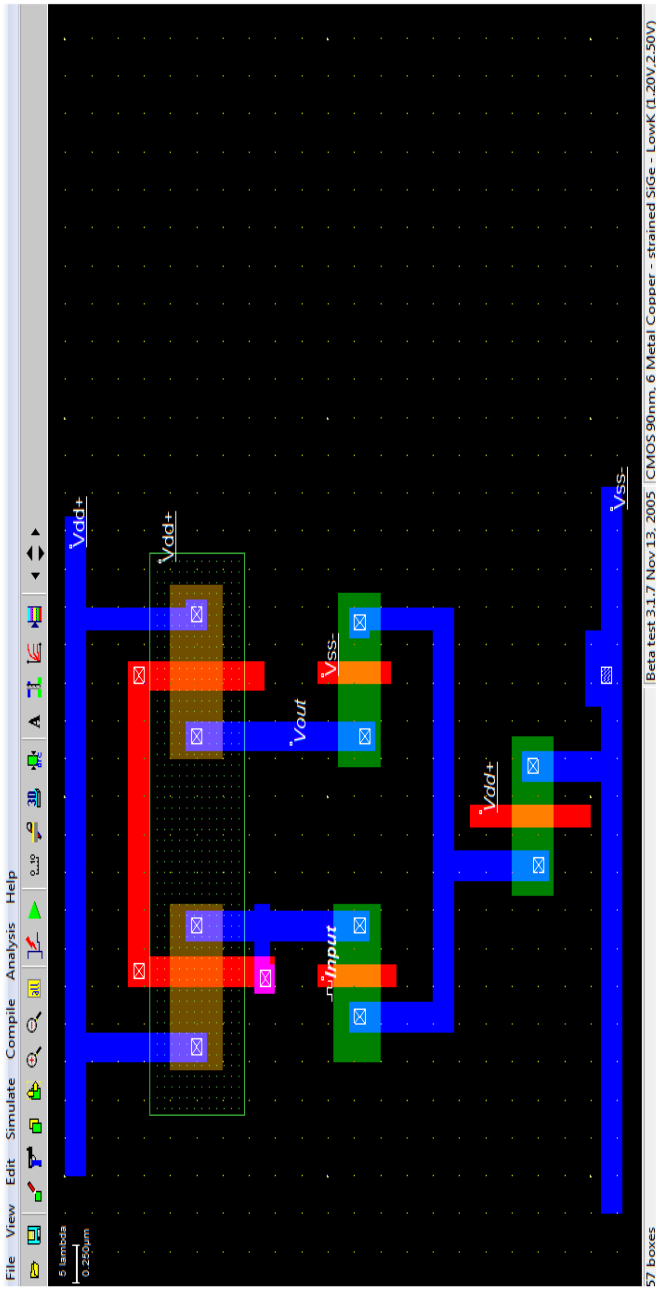

Figure 6: layout of NAF

F. Implementation of Neural Architecture using Analog Components

The components designed in the previous section are used to implement the neural architecture. The tan block is the differential amplifier block designed. This block is used as the neuron activation function as well as for the multiplication purpose.

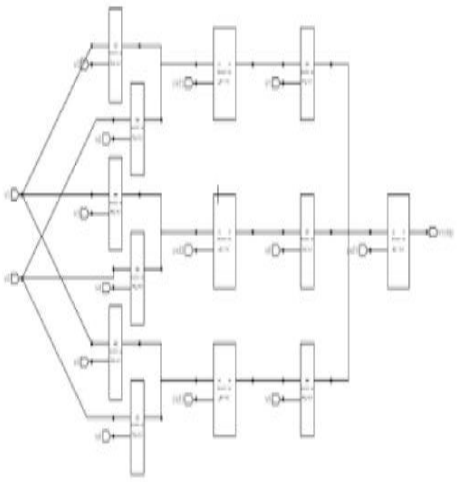

Figure 7: Schematic of Compression Block

Figure 7 shows exactly how the neural architecture of figure 2 is implemented using analog components. The input layer is the input to the 2:3:1 neuron. The hidden layer is connected to then input layer by weights in the first layer. The output layer is connected to input layer. At the last is the output of 2:3:1 neuron. The layout of circuit for signal compression is shown in figure 8.

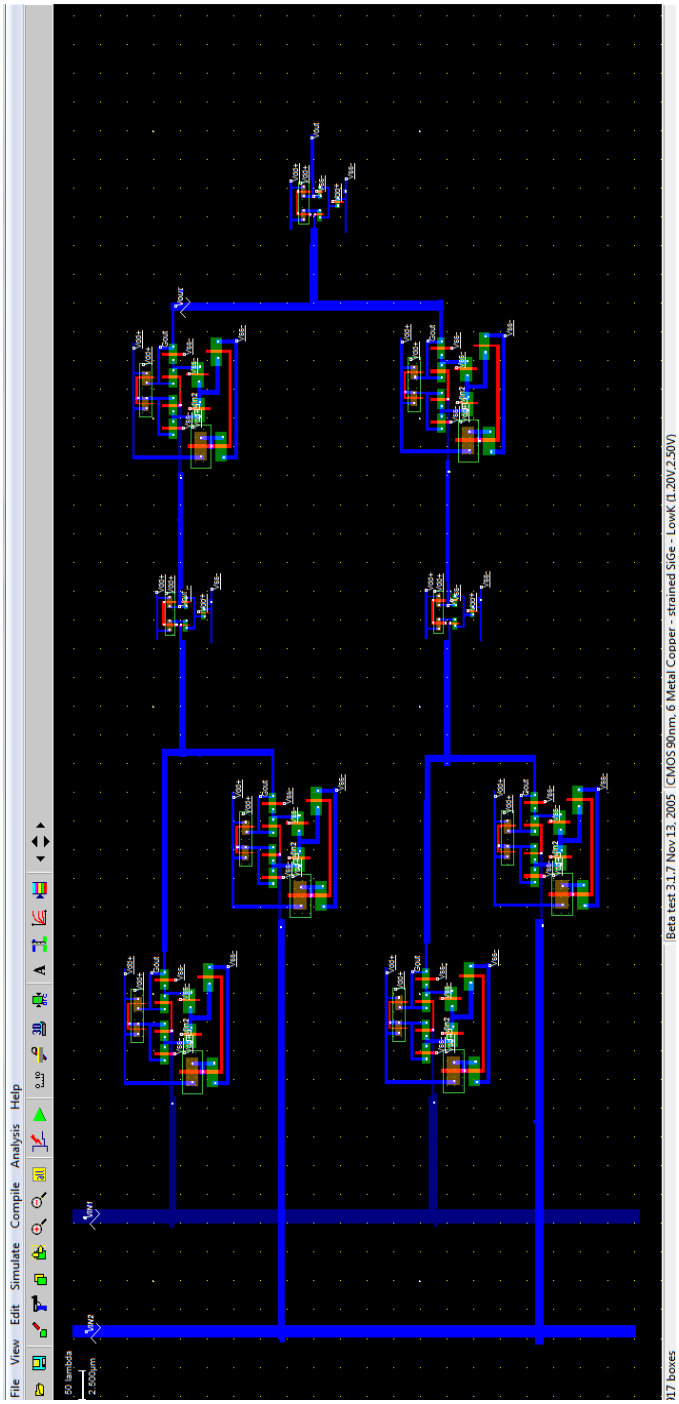

Figure 8: The layout of compression block

III. Application of the Neuron - Signal Compression and Decompression

The above proposed NA is used for signal compression. Signal consisting of pixel intensities are fed to the network shown in Figure 8 for compression and then this compressed signal act as input for the decompression block. The layout of decompression is as shown in figure 10. The 2:3:1 neuron proposed has an inherent capability of compressing the inputs, as there are two inputs and one output. The compression

achieved is **97.30%.** Since the inputs are fed in the analog form to the network there is no need for analog to digital converters.

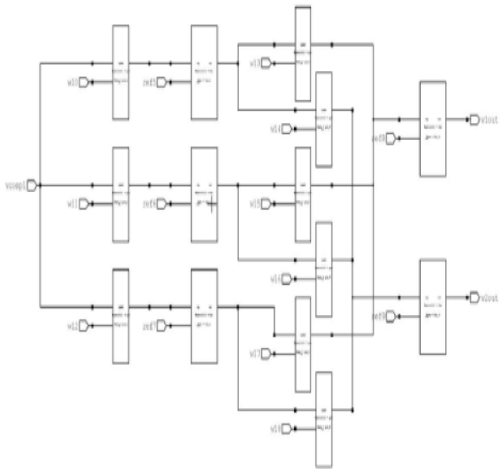

Figure 9: Schematic of Decompression Block

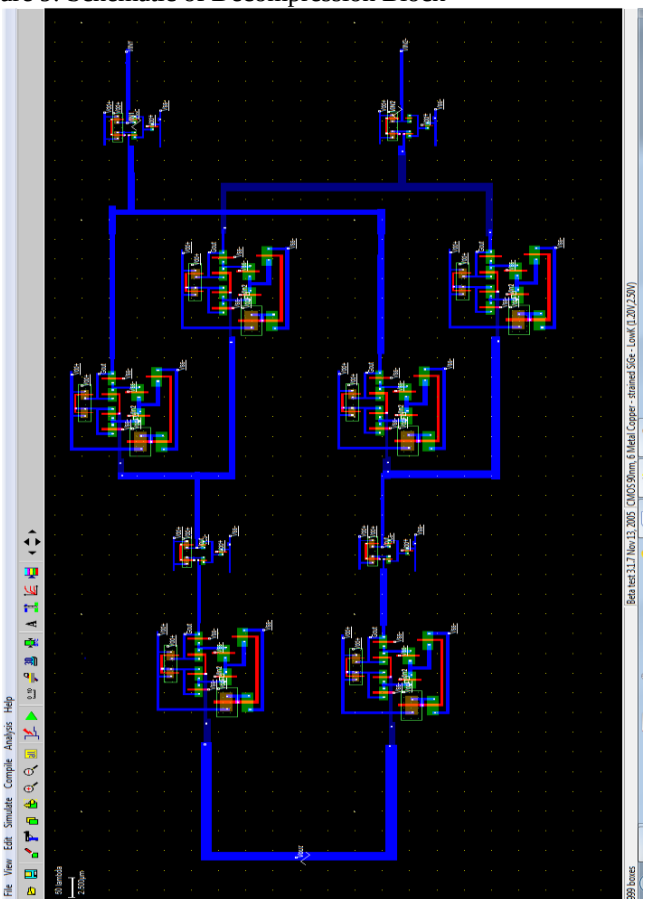

Figure 10: Layout of decompression block**.**

A 1:3:2 neural networks is designed for the decompression purpose. The neural network has 3 neurons in the hidden layer and two in the output layer. Figure 11 shows the compression and decompression scheme. The training algorithm used in this network is Back Propagation algorithm. The error propagates from decompression block to the compression bock. Once the network is trained for different inputs the two architectures are separated and can be used as compression block and decompression block independently

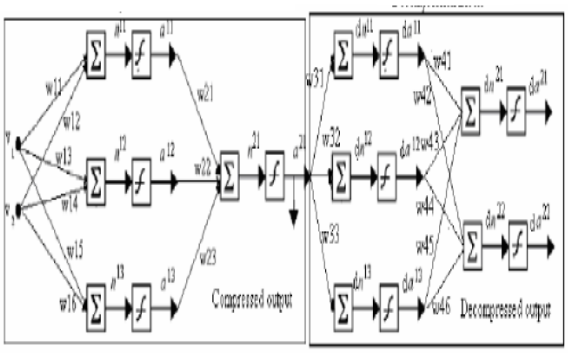

Figure 11: Signal Compression and Decompression using proposed neural architecture

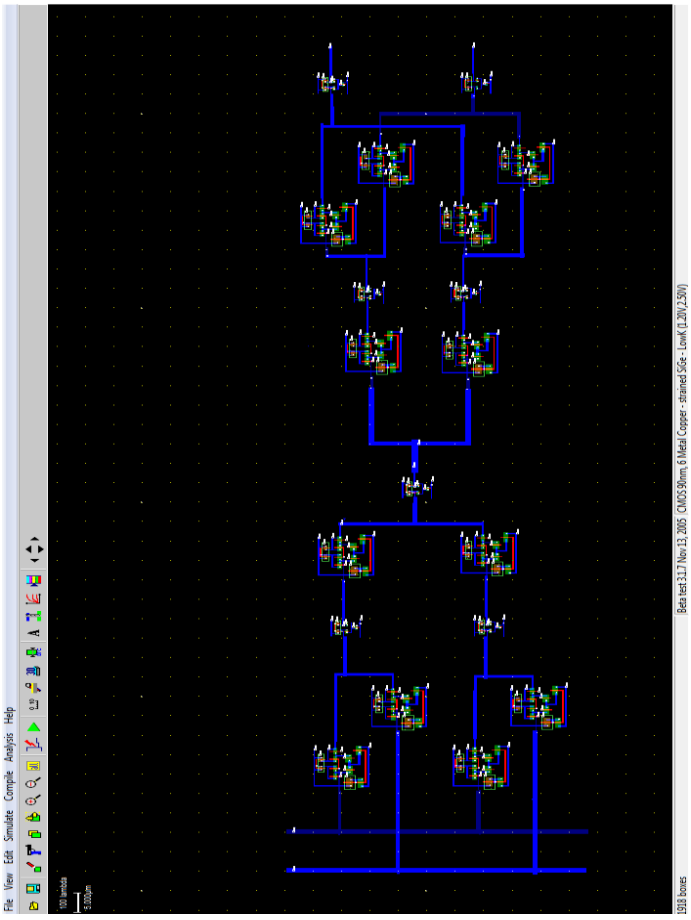

Figure 12: Layout of Signal Compression and Decompression using proposed neural architecture

IV. Back Propagation Algorithm

Back propagation is the most common method of training of artificial neural network so as to minimize the objective function. It is the generalization of delta rule and mainly used for feed forward networks. The back propagation algorithm is

understand by dividing it into two phases. First phase is propagation and second is weight update.

A. Propagation

a) Forward propagation of training patterns input through the neural network in order to generate the propagations output activations.

b) Backward propagation of the of the propagations output activations through the neural network using the training patterns target in order to generate the deltas of all output and hidden in neurons.

B. Weight Update

a) For each weight synapse it multiply its output delta and input activation to get the gradient of the weight.

b) Bring the weight in opposite direction of the gradient by subtracting a ratio of it from the weight.

This ratio influences the speed and quality of learning and it is called learning rate. The sign of the gradient of a weight indicates where the error is increasing, that is why the weight must be updated in the opposite direction. These phases goes on repeating until the performance is of the network is satisfactory.

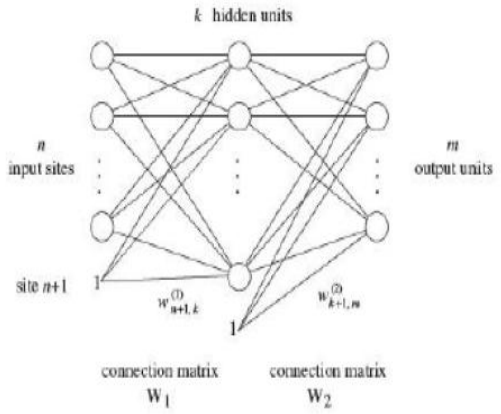

Figure 13: Notation for three-layered network

There are (n + 1) × k weights between input sites and hidden units and (k +1)×m between hidden and output units. Let W1 denote the (n+1)×k matrix with component w ij (1) at the i-th row and the j-th column. Similarly let W2 denote the (k + 1) × m matrix with components wij (2) ij . We use an over lined notation to emphasize that the last row of both matrices corresponds to the biases of the computing units. The matrix of weights without this last row will be needed in the back propagation step. The n-dimensional input vector _ = (o1, . . ., on) is extended, transforming it to ˆo = (o1, . . . , on, 1). The excitation netj of the j-th hidden unit is given by:

$$net_j = \sum_{i=1}^{n+1} w_{ij}^{(1)} \hat{o}_i .$$

The activation function is a sigmoid and the output Oj (1) of this unit is thus

$$o_j^{(1)} = s\left(\sum_{i=1}^{n+1} w_{ij}^{(1)} \hat{o}_i\right)$$

After choosing the weights of the network randomly, the backpropagation algorithm is used to compute the necessary corrections. The algorithm can be decomposed in the following four steps:

(i) Feed-forward computation

(ii) Back propagation to the output layer

(iii) Back propagation to the hidden layer

(iv)Weight updates

The algorithm is stopped when the value of the error function has become sufficiently small.

V. Results and Discussions

A. Simulation Result for Gilbert cell Multiplier

The design Gilbert cell is simulated using 45nm VLSI technology. The simulation result shown in the figure 13 as for the multiplication of the two voltages v1 and v2. Gout is the output of the Gilbert cell multiplier which is the sum of the two outputs voltages i.e 0.24v as shown in figure 11.The power dissipation is 0.58 micriwatt.

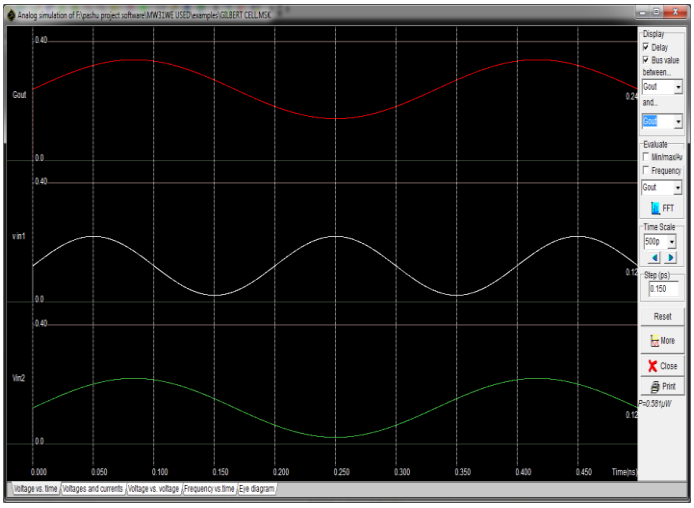

Figure 13: Simulation of gilbert cell multiplier

B. Simulation Result for Neuron Activation Function

The simulation result of neuron activation function is shown in the figure 14. In this NAF we compared the input voltage with reference voltage up till the design work is in sub threshold region which is act as a neuron activation function. The power dissipation of NAF is 0.20 microwatt.

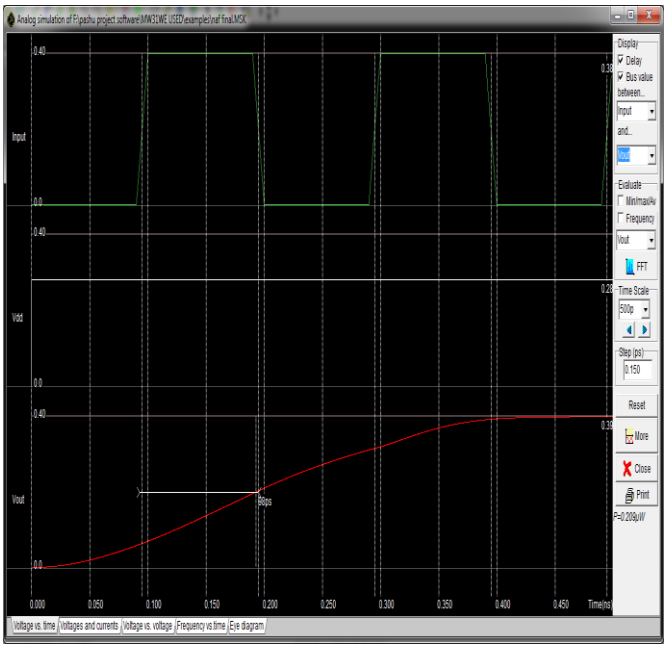

Figure 14: Simulation of NAF

C. Simulation Result for signal compression

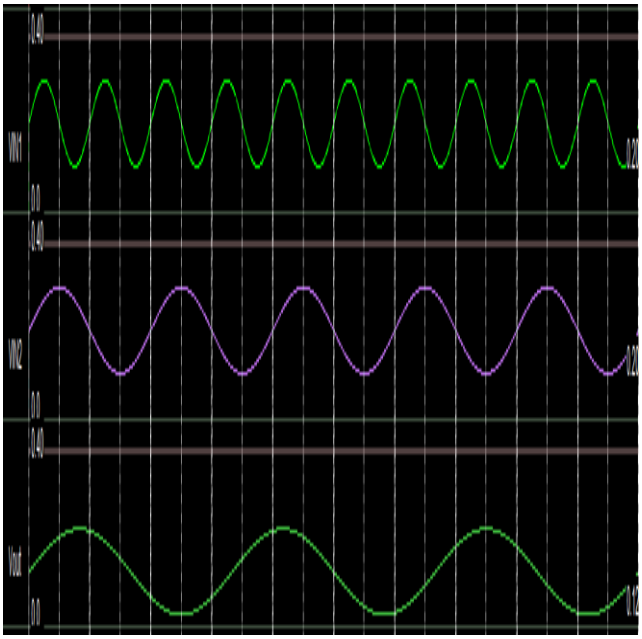

Figure 15: Simulation of signal compression

D. Simulation Result for signal decompression

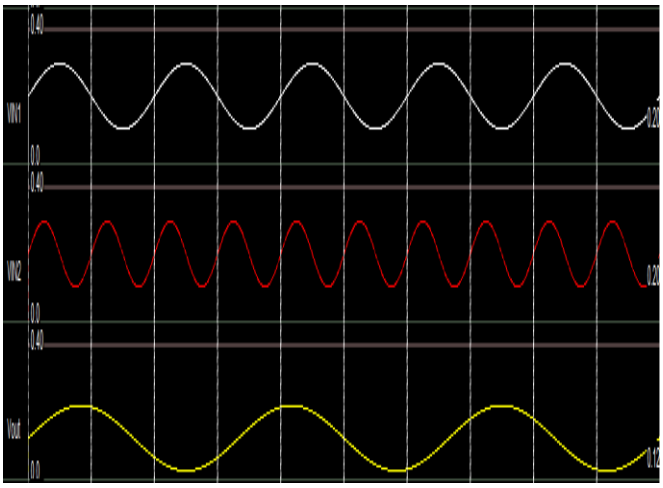

Figure 16: Simulation of signal decompression

E. Simulation Result for signal compression and decompression

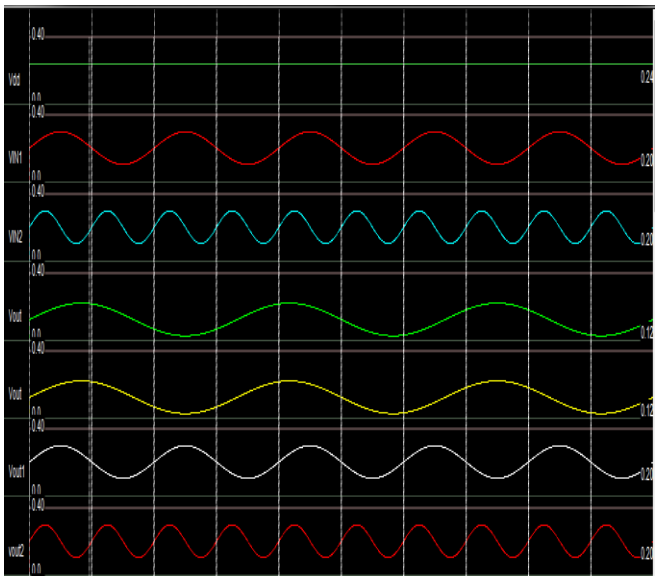

Figure 17: Simulation of signal compression and decompression

From the Figure 17 it is observed that Vin1 and vin2 is the input signal, we compress and decompress the signal and at the output we get the original signals i.e vout1 and vout2.The power dissipation of this signal is 4.60 microwatt. The compression we achieved is 97.22% and average decompression achieved is 60.94%.The main advantages of this neural network architecture is the inputs are fed in the analog form to the network there is no need for analog to digital converters. This is one of the major advantages of this

work, Power consumption, Exact output, high stability i.e accurate output, Minimization of leakage current

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