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DESIGN OF RAIL TO RAIL OPERATIONAL AMPLIFIER USING CMOS

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***Abstract*— A low power CMOS rail to rail op-amp. We realizes in SCNO 180nm technology under 1.8 power supply voltage. A constant trans-conductance is ensured for the whole common-mode input range. The class AB output stage also has a full voltage swing. The circuit provides a gain bandwidth of 16.9-MHz and a DC gain of 81.27 dB. The input transistors operate in weak inversion, which have big gm/Id value, so the power consumption is reduced.**

***Index Terms*— OP-AMP, CMOS, Transient Step Response.**

I. INTRODUCTION

With the development of wireless communication from the second generation (2G) to 3G, many communication standards, such as GSM, TD-SCDMA, WCDMA and CDMA2000 will co-exist for a long time. This phenomenon will also happen in navigation and broadcast television, as there are also many standards, for example: GPS, Galileo, CMMB, DVB-H and so on. So, the reconfigurable radio frequency integrated circuit (RFIC) and broadband data conversion circuit facing multi-standard and multimode wireless communication is very important. For the key part of this circuit, i.e. the RF front-end transceiver, the often taken structure is the zero-intermediate frequency scheme, as there is no image-rejection problem, and consumes less power. The operational amplifier (Op-amp) we proposed is supposed to be used between the down converter and the second stage ADC in the receiver end, and between DAC and the up-converter in the transmitting end. As the Op-amp has both input and output dynamic range rail-to-rail, we can lower requirement for ADC and DAC, thus to improve system performance. Also, battery powered device for communication such as cell phones drives IC to the low power. In this case, designing low-power That is, rail-to-rail. To ensure this, the minimum supply voltage should be Op-amp becomes the fundamental job of designing low-power analog and mixed signal systems. To reach the rail-to-rail amplitude, the input stage and the output stage should be designed respectively.

We can optimize the input stage constant-gm operation by controlling of the total input current. In fact, as we know, in bipolar process and in MOS weak inversion, the gm is proportional to the current, while in MOS strong inversion it is proportional to the square root of the current..For the high supply voltage, there are some ways to make gm constant. One of the often used ways is 1:3 current mirror. Our main goal is to realize a constant gm input stage and a rail-to-rail output stage for a low-power operational amplifier. This has been achieved by the current-switch trans-conductance control circuit in the input stage and the improved class AB in the output one. The paper is organized as follows. The input and the output part will be introduced and analyzed results are verified.

II. PROPOSED METHOD

The basic equations and parameters are described below. These design main parameters are: , phase margin (MΦ), gain-bandwidth product (fGBW), load capacitance (CL), slew rate (SR), input common mode range (ICMR),In this circuit replacing the current source and uses PMOS active load.
Using formula in current and resister and accepted ratio

$$R = 1/K' S(VGS-VT) \quad (1)$$

Where $S=W/L$
$K'=\mu 0COX$
The equations for determining the various Op-Amp characteristics can be shown as follows:

A. Gain and Bandwidth

According to the equivalent circuit shown in Figure 2 under typical conditions
The dc gain of op-amp is given by

$$A=20 \log V0/VIN \quad (2)$$

By placing differential pair M1, M2, M3,M4. It is possible to obtain rail to rail input stage.

B. Common Mode range

If we define VCM as the op-amp input common
Mode range i.e

$$VCM+= VDD- VCM(max) \quad (3)$$

And

$$VCM- = VCM(min) – VSS \quad (4)$$

C. Internal Slew Rate

The slew rate associated with CC is found to be

$$SR = \frac{I_{D5}}{C_C} \quad (5)$$

D. External Slew Rate

The slew rate associated with CL is found to be

$$SR = \frac{I_{D7} - I_{D5}}{C_L} \quad (6)$$

Combining both above equations we obtain

$$I_{D7} = SR(C_C + C_L) \quad (7)$$

DESIGN STEPS FOR TWO-STAGE OP-AMP

In this work, an Op-Amp has been designed which exhibits high unity gain frequency for optimized balancing of phase margin, gain, power, and load. A method is proposed to set a higher unity gain frequency of the Op-Amp working at a lower supply voltage. This allows the value of each circuit element of the amplifier (i.e. transistor aspect ratios, bias current and compensation capacitor) to be univocally related to the required electrical parameters.

Here we have chosen a simple differential pair amplifier for input amplifier, common source amplifier (high gain, swing balancing) for output amplifier, a current mirror circuit and a biasing circuit, and connecting PMOS load in input (replacing current source) with a Miller capacitance in series with each other. We see that simulate in above circuit and get DC Gain 54db and GBW 18.15 MHZ. Then we connected same W/L ratio in series PMOS and NMOS IN Load.

A design steps for two-stage op-amp in Figure 3 can be constructed as follows.

A design steps for two-stage op-amp in Figure 3 can be constructed as follows.

Step1- we have-

$$C_C = \frac{4KT}{3\omega_u A_M(f)}\left[1 + \frac{SR}{\omega_u(V_{GS1}^{eff} - V_{TH})}\right] \quad (8)$$

Step2-I_{D7} is given as-

$$I_{D7} = SR(C_C + C_L) \quad (9)$$

Step-3 The value of L_6 is given by-

$$L_6 = \sqrt{\frac{8}{2}\frac{\mu_p V_{GS6}^{eff^2} C_C}{\omega_u(C_C + C_L)\tan(\Phi_M)}} \quad (10)$$

Step-4 $(W)_6$ is given as-

$$W_6 = \frac{2SR(C_C + C_L)}{\mu_p C_{ox}(V_{GS6}^{eff})^2} L_6 \quad (11)$$

Step-5 I_{D5} is given by

$$I_{D5} = C_C SR \quad (12)$$

Step-6 $(W/L)_{1,2}$ is given as-

$$\left(\frac{W}{L}\right)_{1,2} = \frac{\omega_u^2 C_C}{\mu_n C_{ox} SR} \quad (13)$$

Step-7 The value of $\left(\frac{W}{L}\right)_{3,4}$ is given by-

$$\left(\frac{W}{L}\right)_{3,4} = \frac{2SRC_C}{\mu_n C_{ox}\left(V_{GS1}^{eff} - V_{TH} - \frac{SR}{\omega_u}\right)^2} \quad (14)$$

Step-8 Calculate $(W/L)_7$ from the basic relation $(I_{D7}/I_{D5}) = ((W/L)_7/(W/L)_5)$ yields

$$\left(\frac{W}{L}\right)_7 = \left(\frac{C_C + C_L}{C_C}\right)\left(\frac{W}{L}\right)_{3,4} \quad (15)$$

Step-9 $(W/L)_{5,6}$ is given by

$$\left(\frac{W}{L}\right)_{5,6} = \frac{\left(\frac{W}{L}\right)_6}{2\left(\frac{W}{L}\right)_7}\left(\frac{W}{L}\right)_{3,4} \quad (15)$$

Step-10 Using equation 3.22, 3.3, 3.14 and the triode equation we the find value of R_C as-

$$R_C = \frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_6 V_{eff7}} \quad (17)$$

Where $V_{eff7} = V_{DD} - V_{GS1}^{eff^2} - 2|V_{TP}|$

So $(W/L)_9$ is given as-

$$(W/L)9 = \frac{2C_C SR}{\mu_p C_{ox} V_{GS1}^{eff^2}(V_{DD} - V_{GS1}^{eff^2} - 2|V_{TP}|)} \quad (18)$$

.

By placing two complementary differential pairs in parallel as shown in Fig. 4, it is possible to obtain a rail-to-rail input stage. The NMOS pair is conduction for high input common-mode voltages, in particular

If,

$$V_{SS} + V_{gsn} + V_{dsat} < V_{common} \quad (19)$$

While the pMOS pair is in conduction for low input common-mode voltages

$$V_{common} < V_{DD} - V_{dsat} - V_{sgp} \quad (20)$$

1) Input stage

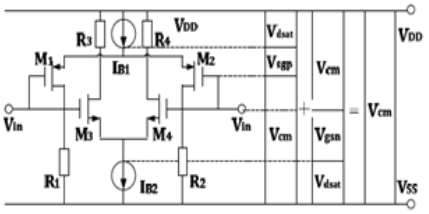

Figure.1. The input range of complementary differential pair

That is, rail-to-rail. To ensure this, the minimum supply voltage should be

$$Vsupmin = Vsgp + Vgsn + Vdsatn + Vdsatp \quad (21)$$

However, a main shortcoming of a rail-to-rail structure is that its total trans-conductance will change. That is, when the input voltage can make both pairs on, its total trans-conductance will be twice of that when only either pair is on. This will bring to the change of the loop gain and thus cause distortion. What's worse? It will decrease phase margin and make the Op-amp unstable.

As the transistors in the proposed circuit work in weak inversion, their trans-conductance are proportional to the currents in them

$$g_{mi\ weak} = I_p/2n_pV_T+I_n/2n_nV_T \quad (22)$$

Where, Ip and I_n are the current in the PMOS and NMOS pair, n_p and n_n are slope factors of the weak inversions. V_T is the thermal voltage. So, to make gm constant, we can tune the current within the input range

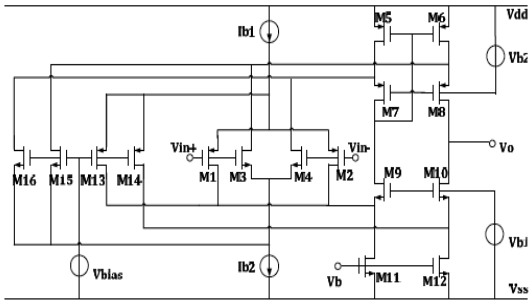

Figure.2. Current switch trans-conductance control circuit**,**

As can be seen from Equation (21) and Fig. 2, we set V_{bias} voltage to be 0.9 V. When the input voltage is low enough, PMOS differential pair M1 and M2 are on while NMOS Differential pair M3 and M4 are off. Then, I_{b1} will come through M1 and M2, I_{b2} will come through M15 and M16, and so the total *g*m will be

$$g_m = g_{mp} = Ip/2n_pV_T \quad (23)$$

When the input voltage is high enough, NMOS transistorsM3 and M4 are on while PMOS transistors M1 and M2 are off.Ib1 will pass through M13 and M14 while *I*b2 though M3 andM4, thus the total *g*m will be

$$g_m = g_{mn} = I_n/2n_nV_T \quad (24)$$

When the input voltage is in the middle range, both pairs are on, the current switch M13, M14, M15, M16 will take away some of the current from Ib1 and Ib2, thus the total gm will be

$$g_m = g_{mp}+g_{mn} = I_p/2n_pV_T + I_n/2n_nV_T \quad (25)$$

Suppose the input voltage is 0.9 V, here MM4 will take 1/4 of the tail current, the expression will be

$$g_m = I_p/4n_pV_T + I_n/4n_nV_T \quad (26)$$

To have gm constant, we should modif1~
y transistor size to make

$$Ip/n_p = I_n/n_n \quad (27)$$

Here the input stage delivers a constant output current to the summing circuit, which consist a high-swing current mirror (M5-M8) and common-gate stage (M9,M10). Gain can be improved by raising the tail current, however, to make sure input transistors are in weak inversion, the width and length of input transistors should be improved which at the same time can lower the offset of the circuit

2) Output stage-

In this work, output stage takes the improved feed-forward class AB circuit. For this circuit as shown in Fig. 3, M27 and M28 are the output part. M19 and M20 form a class AB control circuit. Points A and B have a small DC voltage, which can make sure that output transistors will not both be off thus to avoid cross-over distortion, we know

$$V_{gs19} + V_{gs27} = V_{gs22} + V_{gs23} \quad (28)$$

$$V_{gs20} + V_{gs28} = V_{gs25} + V_{gs26} \quad (29)$$

Let M19 and M22, M20 and M25 have the same size, thenVgs27 = Vgs23, Vgs28 = Vgs26. The quiescent current can thus be expressed as

$$Iq = W/L_{27}/W/L_{23}\ I_{21} \quad (30)$$

Here we suppose the currents in M21 and M24 are the same, and the following equation is satisfied

$$(W/L)_{27}/(W/L)_{28}=(W/L)_{23}/(W/L)_{26}= (W/L)_{22}/(W/L)_{25} = (W/L)_{19}/(W/L)_{20} \quad (31)$$

To make the quiescent current stable, M29 and M30 were added as floating current source, so as to bias the class AB control circuit. Here M29 and M30 has two parts to play, one is

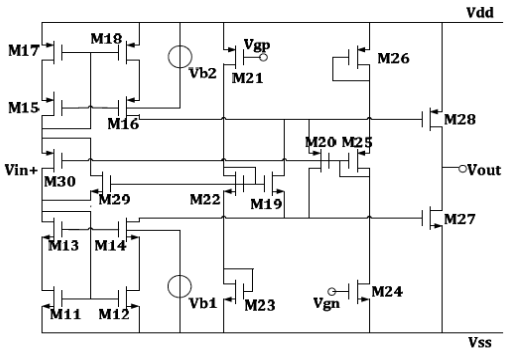

Figure.3. The improved output structure with floating current source

To compensate the effect of voltage source, as they are the same structure of M19 and M20. In this way, PSRR of the circuit can be improved. The second is to make the quiescent current stable, less affected by the common mode input voltage.

The whole circuit can be seen in Fig. 4.

From Fig. 4, we see that the cascaded Miller frequency compensation method was used. Compared to the classical Miller compensation, this method shifts the non-dominant pole to higher frequency.

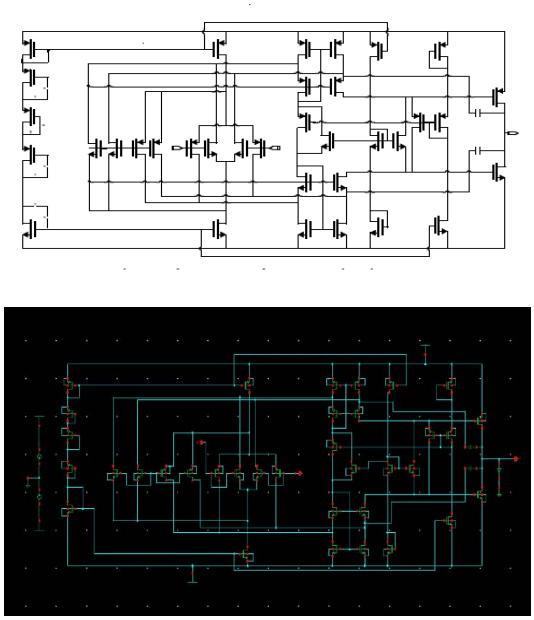

Figure.4. The proposed op-amp circuit

III. SIMULATION RESULT

Based on the proposed circuit in Figure.3 Op-Amp has been designed 180nm CMOS technology. The Op-amp is currently being fabricated in SCNO. So only the post simulation results will be presented here.Fig.4 presents the simulated results of for *V*dd=1.8V. The process parameter and the electrical specification of CMOS op-amp for 180 nm CMOS technology are tabulated in the Table I and Table II respectively. Fig. 6 shows the frequency response of the Op-amp for different Vi,cm values. The DC gain (Av0), gain bandwidth product (GBW), and phase margin (PM) better than 99.2 dB, 16.6 MHz and 65.3° respectively has been achieved. Form Fig.6 we can also see that the GBW and PM of this Op-amp remain almost independent of Vi,cm.

Table 1- Electrical specification of cmos op-amp

$\mu C_{ox}/2$: NMOS (A/V^2)	173.9
$\mu C_{ox}/2$: PMOS (A/V^2)	35.0
Vthpmin (volt)	0.37
Vthmax(volt) NMOS	0.50
ICMR(Volt)	1.3
Vdd(volt)	1.8

A. AC RESPONSE

Through AC response we can simulate the schematic to find out the bode plot and phase plot.

In Figure 5, a bode plot and phase plot for 1.8 V, 27° C and C_L = 5 pf is shown. As can be seen, the open loop gain is 62.05 dB, and a phase margin is -13.69°. The unity gain bandwidth is 17.15 MHz and f bandwidth is 1.74 KHz

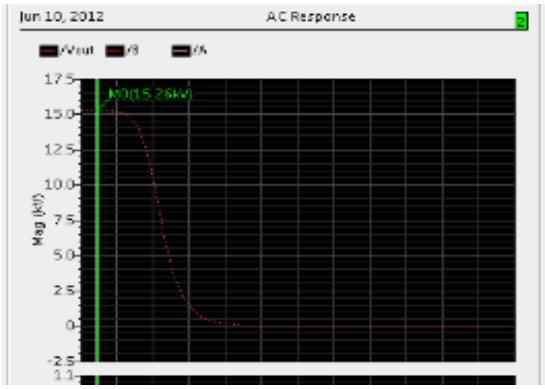

Figure 5.Frequency Response Plot with C_L=5pf

B. TRANSIENT STEP RESPONSE

In Figure 6, a step from ground to V_{DD} is applied at the input with unity feedback configuration.

The slew rate of op-amp is 11.22 V/µS for rising edge of pulse and 11.10 V/ µS for falling edge of the pulse.

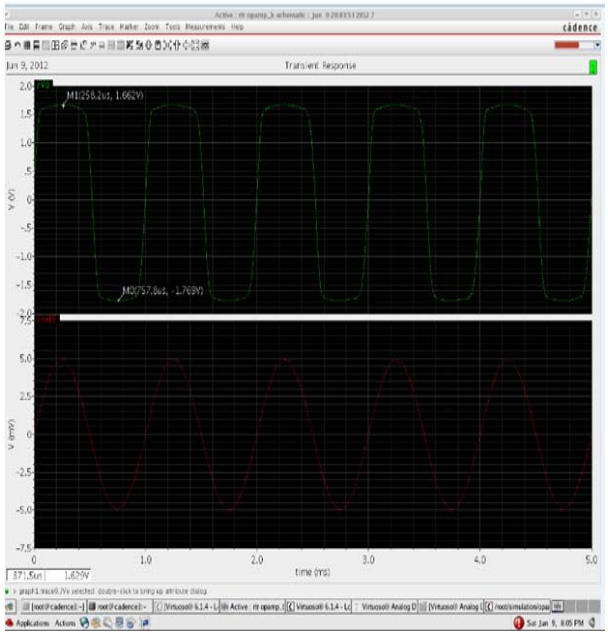

Figure 6.Transient Pulse Response of Op-Amp

C. GAIN AND PHASE

Fig-7 and Fig-8 shows DC gain and Phase .its represent DC gain is 83.67db and phase 136 deg at vdd=1.8 and SCNO 180nm tech.

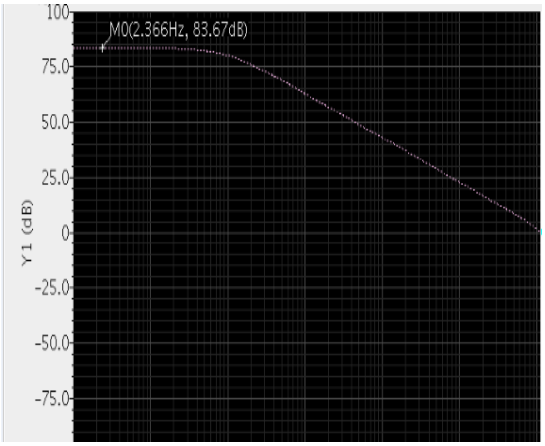

Figure 7 .Dc Gain of Op-Amp

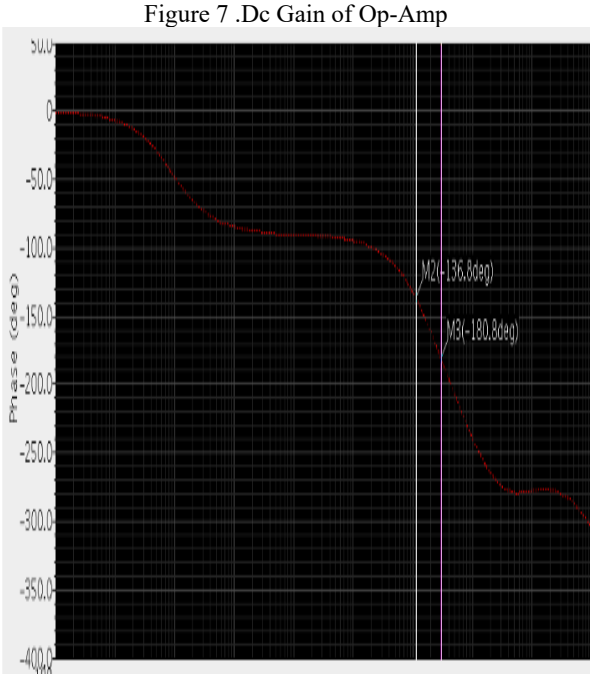

Figure 8 .phase of Op-Amp

D. PHASE AND GAIN MARGIN OF OP-AMP

Phase and gain margin-fig 9 shows that phase margin is 41.6deg and gain margin is 75.6db after simulation in applied voltage 1.8 and gain 83.67db and phase 136.6deg.

Figure 9 .phase and gain margin of Op-Amp

Table 3
Comparison of Simulation Results of two stage and rail to rail class AB control CMOS Op-Amp (180nm Technology)

Specifications	**Simulation results**	**Simulation results**
DC gain (dB)	62.05	81.27
GB (MHz)	18.9	16.9
Phase margin	166.31	152.3
Gain margin	28.36	58.6
CMRR (dB)	159.5	168.8
ICMR (V)	1.3	0.8
Slew rate (V/μS)	11.23	10.20
Power dissipation(μW)	121.4	104.4
I_{D5}(μA)	33.78	14.8
I_{DL}(μA)	140.4	67.1
Load capacitance (pf)	10	5
Supply voltage (V)	1.8	1.8

IV. TEST AND MEASUREMENT

To determine the dc gain improvement provide by the introduce structure. We have realized two stages Op-Amp in 180 nm CMOS technology. In the figures 5 we have simulate it to calculate the transient response, fig-6 shows DC gain, fig-7 phase and fig 8 shows gain margin and phase margin in table 3 we simulate the proposed Op-Amp at 180 nm and measure the performance. By the proposed structure we got excellent result of dc gain and Slew rate. If it is less than the simulated one (not totally realistic, because technology dispersion are not taken into account) dc gain and GBW shows increase DC gain decrease GBW frequency .then I say that yet increase bandwidth of op-amp then balance DC Gain , good being to amplifier. If increase frequency then these amplifier work at oscillator .so we have to balance condition in both. We do not have yet the simulation result for the Op-Amp realized at 180 nm with 1.8 V VDD.

V. CONCLUSION

We simulate the proposed Op-Amp at 180 nm using cadence virtuous and measure the performance. By the proposed structure we got excellent result of dc gain and Slew rate. If it is less than the simulated one (not totally realistic, because technology dispersion is not taken into account) dc gain and GBW shows increase DC gain decrease GBW frequency. Then I say that yet increase bandwidth of op-amp then balance DC Gain, good being to amplifier. If increase frequency then these amplifier work at oscillator .so we have to balance condition in both.

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